INSTRUCTION MANUAL

RACAL-DANA

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The Electronics Group

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1994

UNIVERSAL TIMER/COUNTERS

RACAL-DANA

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RACAL

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Before undertaking any maintenance procedure, whether it be a specific troubleshooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the **WARNING** and **CAUTION** notices contained therein.

The equipment described in this manual contains voltage hazardous to human life and safety and which is capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical hazards and thus prevent personal injury and damage to equipment.

If this instrument is to be powered from the AC line (mains) through an autotransformer (such as a Variac or equivalent) ensure that the common connector is connected to the neutral (earthed pole) of the power supply.

Before operating the unit ensure that the protective conductor (green wire) is connected to the ground (earth) protective conductor of the power outlet. Do not defeat the protective feature of the third protective conductor in the power cord by using a two conductor extension cord or a three-prong/two-prong adaptor.

Maintenance and calibration procedures contained in this manual sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures carefully and heed Warnings to avoid "live" circuit points to ensure your personal safety.

Before operating this instrument:

1. Ensure that the instrument is configured to operate on the voltage available at the power source. See Installation Section.

2. Ensure that the proper fuse is in place in the instrument for the power source on which the instrument is to be operated.

3. Ensure that all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If at any time the instrument:

- Fails to operate satisfactorily
- Shows visible damage
- Has been stored under unfavorable conditions
- Has sustained stress

It should not be used until its performance has been checked by qualified personnel.

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ADDENDUM

RACAL-DANA MODEL 1994, OPTION 01

Addition to p. 1-15, Table 1.1 Specifications:

Option 01, Rear Panel Inputs

Inputs A and B

Sensitivity at rear panel inputs is as specified on pp. 1-6 and 1-7.

Sensitivity at front inputs is not specified and will be degraded.

The following statement must be added to the following procedures:

p. 6-21, under NOTE in step (6) of paragraph 29

p. 6-23, under NOTE after step (7) of paragraph 33

p. 6-26, step (2) of paragraph 44

p. 6-27, step (1) of paragraph 45

p. 6-27, step (2) of paragraph 47

p. 6-28, step (1) of paragraph 48

p. 6-31, step (1) of paragraph 56

p. 6-32, step (2) of paragraph 58

p. 6-35, step (2) of paragraph 62

Procedure must be performed on rear inputs when Option 01 is installed.

August 1993

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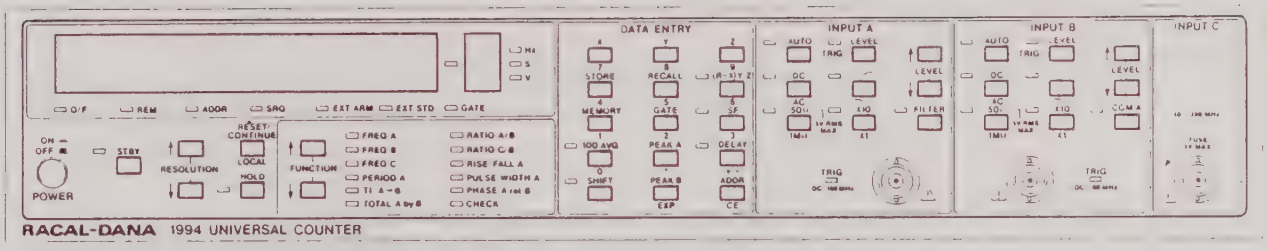


Figure 1.1 - Model 1994 Universal Timer/Counter

SECTION 1 GENERAL INFORMATION

1.1 INTRODUCTION

1.1.1 The Racal-Dana universal counter Model 1994 is a microprocessor-controlled instrument offering high accuracy measurements with a comprehensive range of capabilities. The 1994 can be provided with Option 41 Input C, extending frequency measurement to 1.3 GHz.

1.2 MEASUREMENT FUNCTIONS

1.2.1 Frequency A and B

1.2.1.1 Frequency A and B are used to measure the frequency of the signal applied to Inputs A and B, respectively. A resolution of 9 digits is available with a 1-second gate time.

1.2.2 Frequency C

1.2.2.1 Frequency C is available as Option 41. A resolution of 9 digits is available with a 1-second gate time.

1.2.3 Period A

1.2.3.1 Period A is used to measure the period of the waveform applied to Input A. A resolution of 9 digits is available with a 1-second gate time.

1.2.4 Time Interval

1.2.4.1 Time Interval provides single-shot measurements of the time interval between:

1. Separate Mode: An event occurring at Input A and a later event at Input B
2. Common Mode: Two events occurring at Input A

1.2.4.2 The arming of the stop trigger circuit can be delayed to prevent the measurement interval being stopped prematurely by spurious pulses, such as those caused by contact bounce.

1.2.5 Total A by B

1.2.5.1 Total A by B permits events occurring at Input A to be totalized. The counting interval can be controlled by:

1. Electrical start and stop signals applied to Input B (Total A by B)
2. Successive operations of a front panel key accumulating counts (Manual Totalize)

1.2.5.2 Delayed arming of the stop circuit to prevent spurious triggering is available in the Total A by B mode.

1.2.6 Ratio A/B

1.2.6.1 Ratio A/B is used to measure the frequency ratio between Inputs A and B.

1.2.7 Ratio C/B

1.2.7.1 When Option 41 is installed, Ratio C/B is used to measure the frequency ratio between Inputs C and B.

1.2.8 Rise/Fall A

1.2.8.1 Rise A and Fall A are automatically measured using positive and negative slope selection, respectively.

1.2.9 Pulse Width A

1.2.9.1 Positive and negative Pulse Widths A are automatically measured using positive and negative slope selection, respectively.

1.2.10 Phase A rel B

1.2.10.1 Phase A rel B is used to measure the phase difference between the waveform applied to Inputs A and B. The phase difference is displayed in degrees, and indicates the phase lead at Input A.

1.2.11 Check

1.2.11.1 The Check function enables a number of functional tests of the instrument's circuits to be made without the use of additional test equipment. For example, the 1994 can measure its own 10 MHz internal reference standard. Although these tests do not check the instrument's performance to published specifications, they can be used to verify that the equipment is operating correctly following receipt or transportation to a new location. The Check function can be extended using special functions (see Subsection 3.4.8) to provide a comprehensive range of self tests.

1.3 SIGNAL INPUT CHANNELS

1.3.1 Inputs A and B are fully independent, but provision is made for connection of Input A's signal into both channels (common mode). When this is done, Input B's socket is isolated from Channel B.

1.3.2 Both Inputs A and B are provided with independent controls to permit selection of:

1. AC or DC input coupling
2. 1MΩ or 50Ω input impedance
3. X1 or X10 input attenuation
4. Positive or negative-slope trigger
5. Manual or automatic setting of input trigger level

1.3.2.1 The manually set trigger level is entered into an internal store.

1.3.2.2 The auto-trigger level is derived by measuring the positive and negative peaks of the input signal. If the peak-to-peak value exceeds 5.1V, or if either peak is outside the range ±5.1V, the X10 attenuator is automatically switched-in. The trigger level is then set to the mean of the measured value.

1.3.2.2.1 When operating in auto-trigger with the X10 attenuator in-circuit, the attenuator will be switched-out if the peak-to-peak value is less than 4.6V and both peak values are within the range ±4.6V.

1.3.2.2.2 The trigger levels in use are available at pins mounted on the rear panel. The voltage range is ±5.1V regardless of whether the attenuator is switched-in or out.

1.3.3 Input C has a nominal input impedance of 50Ω and is AC-coupled. Protection against excessive signal levels is provided by a 5V rms fuse in the input BNC connector.

1.4 LOW-PASS FILTER

1.4.1 An internal low-pass filter can be introduced to reduce the bandwidth of Input A to 50 kHz (nominal).

1.5 MATH COMPUTATION

1.5.1 When the Math function is active, the displayed value is (Measurement Result-X) Y/Z where X, Y, and Z are values entered into stores within the instrument by the user. X is set to 0, Y and Z to 1 when the instrument is powered-on. By an appropriate choice of values for X, Y, and Z, offset, normalized, and scaled displays can be achieved.

1.6 SPECIAL FUNCTIONS

1.6.1 The 1994 provides a set of Special Functions, permitting extended measurements and capabilities beyond those provided by the front-panel keyboard. See Subsection 3.4.10 for details.

1.7 ERROR INDICATION

1.7.1 Certain errors in counter operation will result in the display of error codes. See Subsection 3.4.11 for details.

1.8 EXTERNAL ARMING

1.8.1 External arming of the start and stop trigger circuits for the measurement interval can be carried out by means of signals applied to a rear-mounted BNC connector. Any combination of internal and external arming can be selected by use of the appropriate special function.

1.9 DISPLAY FORMAT

1.9.1 The display uses an engineering format, with a 9-digit mantissa and 1-digit exponent. Overflow of the most significant digits can be used to increase the display resolution.

1.10 HOLD

1.10.1 The Hold feature allows readings to be held indefinitely. A new measurement cycle is initiated using the RESET key.

1.11 GATE TIME AND RESOLUTION

1.11.1 Refer to Subsections 3.4.3 and 3.4.4 for details. In Frequency A and B, Frequency C, Period A, Ratio A/B and C/B modes, a gate time may be specified from the front panel (Gate Time mode) or by the selected display resolution using the RESOLUTION (↑↓) keys (Resolution mode). The available gate time range is 1 ms to 99.9 s.

1.11.2 In the Total A by B and Manual Totalize modes, the counting interval (i.e., gate time) is controlled by the time interval between the start and stop signals at Input B, or between successive operations of the HOLD key.

1.11.3 In Phase mode, the gate time is fixed and the display resolution is determined by the input signal frequency.

1.12 EXTERNAL FREQUENCY STANDARD INPUT

1.12.1 The 1994 may be operated using an external frequency standard. The counter will operate from the external standard when a signal of sufficient amplitude is applied at the EXT STD INPUT BNC connector. The counter reverts to internal frequency standard operation automatically if the external standard input is removed.

1.13 STANDBY MODE

1.13.1 When the 1994 is switched to Standby, the internal frequency standard continues to operate but the measuring circuits are switched off.

1.14 GPIB INTERFACE

1.14.1 An IEEE-488-1978 GPIB interface is standard on the 1994. This feature permits remote control of all the instrument's functions except the power ON/OFF and STBY switching. See Section 4 for 1994 system operation.

1.15 OPTIONS AVAILABLE

1.15.1 Rear Panel Input (Option 01)

1.15.1.1 This permits use of rear-mounted Inputs A, B, and C. This is a factory-installed option.

1.15.2 Frequency Standards (Options 04A and 04E)

1.15.2.1 Two internal frequency standard options are available. The technical specifications are given in Table 1.1. The frequency standard can be changed, if necessary, by the customer (see Section 2).

1.15.3 Reference Frequency Multiplier (Option 10)

1.15.3.1 The reference frequency multiplier is a phase-locked multiplier which permits the use of external frequency standard signals at 1 MHz, 2 MHz, 5 MHz or 10 MHz. The multiplier can be installed by the customer; instructions are given in Section 2.

1.15.4 1.3 GHz Input C (Option 41)

1.15.4.1 This provides the 1994 with high-frequency measurement capability to 1.3 GHz.

1.15.5 Fixed-Mount Rack (Option 60)

1.15.5.1 This permits fixed 19-inch full-rack installation of the 1994. See Subsection 2.5.2 for field installation.

1.15.6 Slide-Mount Rack (Option 65)

1.15.6.1 This permits standard 19-inch full rack installation with slides for the 1994. See Subsection 2.5.3 for field installation.

1.16 SAFETY

1.16.1 The 1994 incorporates a protective earth terminal and is designed to meet international safety requirements. Refer to the safety page "FOR YOUR SAFETY" immediately preceding the Table of Contents. Follow all **NOTES**, **CAUTIONS**, and **WARNINGS** to ensure personal safety and prevent damage to the instrument.

1.17 PRODUCT SUPPORT

1.17.1 Racal-Dana supports the 1994 with Product Engineering, Service, and Parts Departments. A complete listing of service centers and field representatives is provided on the last two pages of the manual.

1.18 SPECIFICATIONS

1.18.1 Table 1.1 lists the 1994 specifications. They specify the performance standards to which the instrument should be tested during any necessary calibration and/or servicing.

Table 1.1 - 1994 Specifications

GENERAL DESCRIPTION

The 1994 universal counter provides the following measurement functions: frequency, frequency ratio, period, high-resolution time interval, rise/fall time, pulse width, phase, and totalize. A full talker/listener GPIB is a standard feature. Supplemental features include mathematical manipulation of measurements, averaging of 100 readings, peak amplitude measurement, and a high-speed "raw" data output via the GPIB.

The frequency range on Inputs A and B is DC to 160 MHz; 40 MHz to 1.3 GHz on Input C using a plug-in option board. Single-shot time interval resolution is 1 nanosecond or 9 digits per second of measurement time. Trigger levels on Inputs A and B can be set via the front-panel keypad or via auto-trigger at the 50% point of the input waveform. Trigger levels can be shown on the main display.

A full range of options support the 1994 including rear-panel inputs (Option 01), precision ovenized oscillators (Options 04A, 04E), external frequency standard multiplier (Option 10), 1.3 GHz Input C (Option 41), fixed rack mount (Option 60), and slide rack mount (Option 65). The 1994 is housed in a 3.5-inch, full-width rack chassis.

INPUT CHARACTERISTICS

Inputs A and B

Frequency Range:

DC Coupled	0 to 100 MHz
AC Coupled	10 Hz to 100 MHz

Note: Input A frequency range is 0 to 160 MHz in the frequency mode.

Input Impedance (X1, X10):

High, Separate	1 MΩ shunted by 45 pF (nominal)
High, Common	1 MΩ shunted by 55 pF (nominal)
50Ω, Separate and Common	50Ω (nominal)
Sensitivity, Sine Wave (X1):	25 mV rms to 100 MHz 50 mV rms to 160 MHz (Input A Frequency mode only)

Table 1.1 - 1994 Specifications (Cont'd)

Sensitivity, Pulse (X1):	75 mV p-p; 5 ns min. width 150 mV p-p; 3.1 ns min. width- (Input A Frequency mode only)	
Dynamic Range (X1):	75 mV to 5V p-p; 0 to 50 MHz 75 mV to 2.5V p-p; 50 to 100 MHz 150 mV to 2.5V p-p; 100 to 160 MHz	
Signal Operating Range (X1):	-5.1V DC to +5.1V DC	
Input Attenuation:	X1 or X10, selectable	
Damage Level:		
1 MΩ input impedance	X1:	260V (DC + AC rms), DC to 1.92 kHz $\frac{5 \times 10^5 \text{V rms}}{\text{Frequency (Hz)}}$, 1.92 to 100 kHz 5V rms, 100 kHz
	X10:	260V (DC + AC rms), DC to 19.2 kHz $\frac{5 \times 10^6 \text{V rms}}{\text{Frequency (Hz)}}$, 19.2 to 100 kHz 50V rms >100 kHz
50Ω input impedance	X1, X10:	5V rms, DC to 160 MHz
Triggering:		
Trigger Level	Automatic or manual selection in the +5.1V to -5.1V range (X1), +51V to -51V range (X10). Trigger level readout is shown on main display. Automatic mode: trigger points are set halfway between the max. and min. measured values of the input signal. Input signal must be continuous, with lowest auto-trigger frequency being 50 Hz. Auto-trigger to a DC level is possible. Nominal auto-trigger time is 500 ms per input. Auto-trigger selection of the attenuator is automatic as follows: X1 selected if positive and negative peak amplitudes are $< \pm$ 4.6 and the peak-peak amplitude is $\leq$ 4.6V X10 selected if positive and negative peak amplitudes are $> \pm$ 5.1 or the peak-peak amplitude is >5.1V Manual mode: trigger levels can be entered via the keyboard or using the increment/decrement button	
Trigger Level Setting	20 mV steps, nominal (X1) 200 mV steps, nominal (X10)	

Table 1.1 - 1994 Specifications (Cont'd)

Trigger Level Accuracy	± 1% reading ± 30 mV relative to trigger level set (X1) ± 1% reading ± 300 mV (X10)
Auto-Trigger Minimum Amplitude	150 mV p-p
Auto-Trigger Level Accuracy	± 30 mV relative to displayed reading
Read Peak Amplitude Accuracy	Frequency Range: DC, 50 Hz to 20 MHz X1: ± 50 mV ± 6% Vp-p (sinewave) ± 40 mV ± 1% reading (DC) X10: ± 1% reading ± 500 mV ± 6% Vp-p
Coupling:	AC or DC
Slope:	Positive or negative; independently selectable
Low-Frequency Filter: (Input A only)	50 kHz (nominal)
Input Connections:	BNC sockets
Crosstalk (X1 at 100 MHz):	36 dB between channels, measured using 50Ω input impedance
FREQUENCY MEASUREMENT (INPUTS A and B)	
Range:	
Input A	6×10^{-4} Hz to 160 MHz
Input B	3×10^{-4} Hz to 100 MHz
LSD Displayed:	$\frac{10^{-9} \times \text{Frequency}}{\text{Gate Time}}$
Resolution:	(± 2 x LSD) $\frac{\pm 1.4 \times \text{Trigger Error} \times \text{Frequency}}{\text{Gate Time}}$
Accuracy:	± Resolution ± Timebase Error x Frequency
PERIOD A MEASUREMENT	
Range:	6.25 ns to 1.7×10^{3} s
LSD Displayed:	$\frac{10^{-9} \times \text{Period}}{\text{Gate Time}}$ (see note 1)

Table 1.1 - 1994 Specifications (Cont'd)

Resolution:	$(\pm 2 \times LSD) \pm \frac{1.4 \times \text{Trigger Error} \times \text{Period}}{\text{Gate Time}}$ (see note 2)
Accuracy:	± Resolution ± Timebase Error x Period
TIME INTERVAL MEASUREMENT	
Input Configuration:	
Separate:	Input A start/Input B stop, Input B start/Input A stop (via Special Function 21)
Common:	Input A start/Input A stop
Time Range:	-2 ns to 8 x 10^5s (i.e., stop signal can occur up to 2 ns before the start signal)
Trigger Slopes:	Start, positive or negative Stop, positive or negative
LSD Displayed:	1 ns (100 ps using averaging)
Resolution:	± LSD ± 1 ns rms ± start trigger error ± stop trigger error (see note 2)
Accuracy:	± resolution ± timebase error x TI ± trigger level timing error (see note 2) ± trigger level setting error (see note 2) ± 2 ns (i.e., differential channel delay error - see note 2)
TOTALIZE A BY B	
Input Channel:	Input A (100 MHz max. frequency)
Maximum Rate:	10^8 events/s
Range:	1 to 10^{18} -1
Pulse Width:	5 ns min. at trigger points

Table 1.1 - 1994 Specifications (Cont'd)

Start/Stop:	Input B (electrical) Start, positive; Stop, negative with positive pulse Start, negative; Stop, positive with negative pulse Hold button enabled by Special Function 61 (manual totalize)
LSD Displayed:	± 1 count
Resolution:	LSD
Accuracy:	LSD
FREQUENCY RATIO MEASUREMENT	
Ranges: Ratio A/B	
Input A	DC to 100 MHz
Input B	DC to 100 MHz
LSD Displayed:	$\frac{10 \times \text{Ratio}}{F_A \times \text{Gate Time}}$
Resolution:	$\pm$ LSD $\pm \frac{\text{Trigger Error B}}{\text{Gate Time}}$
Accuracy:	± Resolution
Note: Higher frequency is assumed to be applied to Input A.	
Ranges: Ratio C/B	
Input C	40 MHz to 1.3 GHz/64
Input B	DC to 100 MHz
LSD Displayed:	$\frac{640 \times \text{Ratio}}{F_C \times \text{Gate Time}}$
Resolution:	$\pm$ LSD $\pm \frac{\text{Trigger Error B}}{\text{Gate Time}}$
Accuracy:	± Resolution
Note: Higher frequency is assumed to be applied to Input C.	

Table 1.1 - 1994 Specifications (Cont'd)

RISE/FALL TIME*	
*requires a continuous signal.	
Rise Time (Default State):	Start: positive slope, 10% trigger point Stop: positive slope, 90% trigger point
Fall Time:	Start: negative slope, 90% trigger point Stop: negative slope, 10% trigger point
Input Channel:	Input A
Range:	20 ns to 20 ms
Min. Pulse Height:	500 mV p-p
Min. Pulse Width:	20 ns at signal peaks
LSD Displayed:	1 ns (100 ps using averaging)
Resolution:	± LSD ± 1 ns rms ± start trigger error ± stop trigger error (see note 2)
Accuracy:	± resolution ± trigger level timing error (see note 2) ± trigger level setting error at 10% trigger point ± trigger level setting error at 90% trigger point (see note 2) ± 2 ns (differential channel delay error - see note 2) ± timebase error (see note 2) x rise/fall time

PULSE WIDTH*	
*requires a continuous signal	
Positive Pulse Width: (Default State)	Start: positive slope, 50% trigger point Stop: negative slope, 50% trigger point
Negative Pulse Width:	Start: negative slope, 50% trigger point Stop: positive slope, 50% trigger point
Input Channel:	Input A
Range:	5 ns to 20 ms
Minimum Pulse Height:	150 mV p-p
LSD Displayed:	1 ns (100 ps using averaging)
Resolution:	± LSD ± 1 ns rms ± start trigger error ± stop trigger error (see note 2)

Table 1.1 - 1994 Specifications (Cont'd)

Accuracy:	± resolution ± trigger level timing error (see note 2) ± trigger level setting error (see note 2) ± 2 ns (differential channel delay error - see note 2) ± timebase error (see note 2) x pulse width
PHASE A RELATIVE TO B*	
*requires a continuous signal	
Range:	0.1° to 360°
LSD Displayed:	0.1° to 1 MHz 1.0° to 10 MHz 10.0° to 100 MHz
Resolution:	+ LSD $\frac{(\pm \text{ TI Resolution})}{\text{Period A}} \times 360^{\circ}$
Accuracy:	± LSD $\frac{(\pm \text{ TI Accuracy})}{\text{Period A}} \times 360^{\circ}$
MATH	
Applies to all counting/timing measurement functions. Note that the Math function is applied prior to the Statistics function.	
Display:	$\frac{\text{Reading} - X}{Z}\ Y$ where X, Y, and Z are constants entered and stored via the keyboard. The displayed measurement reading can also be stored.
Constant (X, Y, or Z) Range:	$\pm 1 \times 10^{-9}$ to $\pm 10 \times 10^{9}$ to nine significant figures
Note: Any number exceeding this range will result in a displayed Op Er.	
Display Range:	± 999.999999 E ± 9
AVERAGE MODE	
Number of Samples:	100 measurements are accumulated and averaged for display
Note: The Average mode applies to all functions except totalize.	

Table 1.1 - 1994 Specifications (Cont'd)

GATE TIME	
Range	200 µS to 99.9S
Resolution:	25.6 µs
TIME INTERVAL DELAY	
Range:	200 µS to 800 mS
Step Size:	25.6 µs, entered via keyboard
Accuracy:	± 50 µs ± 0.1% reading
BASIC FREQUENCY STANDARD	
Internal Frequency:	10 MHZ
Adjustment Range:	± 5 ppm min. at shipment, by single turn trimmer via rear panel
Aging:	
Initial	1 ppm/month at shipment
Long Term	2 ppm/first year
Temperature Stability:	± 10 ppm over the range 0° to 50 °C, referenced to 25°C
External Standard Input:	
Frequency	10 MHz
Level	Min., 100 mV rms; Max., 10 V rms
Max. Input Level	400V peak to 500 Hz, decreasing to 10V rms at 30 kHz and above
Impedance	1 kilohm (nominal) for signals <1V p-p, decreasing to 500 ohms (nominal) for signals 10V p-p and above. AC coupled
Note: The external reference multiplier (Option 10) may be used to lock other standard frequencies that are subharmonics of 10 MHz.	
Internal Standard Output:	
Frequency	10 MHz
Level	≃600 mV p-p into 50 ohms

Table 1.1 - 1994 Specifications (Cont'd)

EXTERNAL ARMING

Applicability:	All functions, except phase, can be armed by rear-panel input with modes selected by front-panel entered special function
Input Signal:	
Sensitivity	500 mV p-p
Offset	+4 to -4V (potentiometer adjusted)

Arming Mode:

1.	Start-Off	Stop-Off	SF10 (Default)
2.	Start-⎍	Stop-Off	SF11
3.	Start-⎏	Stop Off	SF12
4.	Start-⎍	Stop- ⎍	SF15
5.	Start-⎏	Stop- ⎍	SF17
6.	Start-⎍	Stop- ⎏	SF16
7.	Start-⎏	Stop- ⎏	SF18

Note: "Off" state indicates the counter's self-arm start/stop is used.

Minimum Start-Stop Arm Period: 100 ns

GATE OUT

A TTL-compatible signal (into 1 kilohm) is provided from a rear-panel BNC connector coincident with the measurement gate. The signal level is low while the gate is open

NON-VOLATILE MEMORY

Up to ten complete front-panel settings (including math function stores) may be retained for subsequent recall

GPIB INTERFACE

Standard:	IEEE-STD-488-1978
Programmable Controls:	All front-panel keyboard controls except power on/off and standby
IEEE-488 Subsets:	SH1, AH1, T5, TE0 (none), L4, LE0 (none), SR1, RL1, PP0 (none), DC1, DT1, C0 (none), and E2 (3-state bus drivers)

Table 1.1 - 1994 Specifications (Cont'd)

Handshake Time: (DAV to NDAC)	7 µs to 90 µs, typical, depending on the interface message
Data Output Rate:	150 readings/s in high-speed output mode 15 readings/s in normal output mode
Data Output Format:	
High-Speed Output mode	19 binary bytes containing event counts, time counts, TEC (timing error correction) counts, and calibration constants
Normal Output mode	FF+/-D.DDDDDDDDDDE+/-DDCRLF Where: FF are ASCII characters identifying function; D is an ASCII digit; and the decimal point varies within the mantissa
TEMPERATURE PERFORMANCE	
Operating Temperature:	$0^{\circ}C$ to $50^{\circ}C$
Storage Temperature:	$-40^{\circ}C$ to $+70^{\circ}C$
POWER REQUIREMENTS	
These include 100, 120, 220, and 240V rms ± 10%, 45 to 450 Hz ± 10%, 35 VA approximately	
DIMENSIONS	
These include 89 mm (3.5 in) High x 427 mm (16.8 in) Wide x 345 mm (13.6 in) Deep	
WEIGHT	
Approximately 6 kg (13.2 lb)	
OPTIONS	
Option 01 Rear Panel Inputs	
Option 04A High-Stability Oven Oscillator	
Fast warm-up, ovenized Internal Frequency Standard	
Frequency:	10 MHz
Aging:	$<1 \times 10^{-8}$/day at shipment averaged over ten days
	3×10^{-9}/day averaged over 10 days continuous operation
Temperature Stability:	$<1 \times 10^{-7}$ (frequency at $25^{\circ}C$) over the range 0° to $50^{\circ}C$
Line Voltage Stability: change	$<5 \times 10^{-9}$ two minutes after a 10% line voltage

Table 1.1 - 1994 Specifications (Cont'd)

Option 04E High-Stability Oven Oscillator

Proportionally-controlled, ovenized Internal Frequency Standard

Frequency:	10 MHz
Aging:	$<5 \times 10^{-10}$/day at shipment
Temperature Stability:	$<7 \times 10^{-9}$ over the range 0° to 50°C
Line Voltage Stability:	$<5 \times 10^{-10}$ two minutes after a 10% line voltage change

Option 10 External Frequency Standard Multiplier

Phase-locked frequency multiplier enabling 1, 2, 5, or 10 MHz to be used as the external standard

Frequency Input:	1, 2, 5, or 10 MHz ± 10 ppm
Signal Level:	100 mV rms sinewave min., 10V rms max.
Maximum Input Levels:	400V peak up to 500 Hz, decreasing to 10V rms at 30 kHz and above
Input Impedance:	1 kilohm (nominal) for signals<1V p-p, decreasing to 500 ohms (nominal) for signals 10V p-p and above. Ac coupled

Option 41 1.3 GHz Input C

Plug-in option extending the counter range to 1.3 GHz

Frequency Range:	40 MHz to 1.3 GHz
Sensitivity, Sine Wave:	Better than 10 mV rms to 1.0 GHz Better than 75 mV rms to 1.3 GHz
Dynamic Range:	10 mV to 5V rms to 1.0 GHz 75 mV to 5V rms to 1.3 GHz
Impedance:	50 ohms (nominal), AC-coupled, VSWR-2:1 at 1 GHz
Maximum Operating Input:	1V rms
Maximum Input: (without damage)	7V rms (fuse-protected, fitted inside input connector)

Table 1.1 - 1994 Specifications (Cont'd)

LSD, Resolution, and Accuracy:	Same as Inputs A and B frequency
Option 60 Rack-Mounting Kit (Fixed)	
Option 65 Rack-Mounting Kit (Sliding)	

DEFINITIONS AND NOTES

1. Resolution and Gate Time

   a. Refer to the table below. The gate time is set by the selected resolution in the frequency, period, ratio, and check functions. However, gate times may also be programmed in increments rounded to the nearest 25.6 µs using the range of 200 µs to 99.999 s. The default state is determined by the resolution selected (see table), and is 100 ms (8 digits) at power-on. Also, the gate time may be extended by:

   - one period of the input signal on Frequency B and Ratio A/B
   - two periods of the input signal on Frequency A and Period A

   b. The resolution of phase and totalize is determined by the input signal

   c. Time interval, rise/fall time, and pulse width measurements have the resolution determined by both the input signal and the resolution set

Resolution (no. of selected digits) in Frequency, Period Ratio, and Check-See Note 1	**Gate Time**	**Display**	**GPIB Code**
9 + Overflow	10 s	Up Stop	SRS* 10
9	1 s		9
8	100 ms	Default	8
7	10 ms		7
6	1 ms		6
5 } See	1 ms		5
4 } Note	1 ms		4
3 } 2	1 ms	Down Stop	3

NOTE 1:

The most significant digit is permitted to exceed the resolution by 1 digit providing a 10% overrange. This precludes unnecessary shifting of digits.

*SRS = Store the Display Resolution Command

Table 1.1 – 1994 Specifications (Cont'd)

NOTE 2:

Measurements of frequency, period, ratio, and check are averaged when these gate times are set.

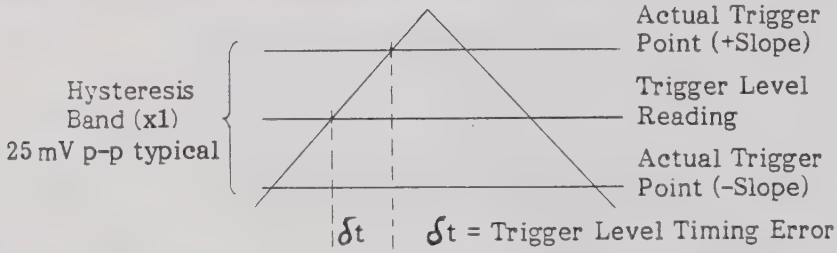
2. Trigger Error

Trigger Error equals $\frac{\text{SQR}(e_i^2+e_n^2) \text{ seconds rms}}{\text{Input Slew Rate At Trigger Point}}$

where e_i = input amplifier rms noise (typically 150 µV rms in 160 MHz bandwidth)

where e_n = input signal rms noise in 160 MHz bandwidth

3. Trigger Level Timing Error (X1)


Actual Trigger Point (+Slope)
Hysteresis Band (x1) 25 mV p-p typical
Trigger Level Reading
Actual Trigger Point (-Slope)
δt
δt = Trigger Level Timing Error

$$\text{TIMING ERROR} = \frac{1/2 \text{ Hysteresis Band}}{\text{Input Slew Rate at START Trigger point}} - \frac{1/2 \text{ Hysteresis Band}}{\text{Input Slew Rate at STOP Trigger point}}$$

4. Differential Channel Delay Error

A system error, typically less than 1 ns, but which can be compensated by numerical offset or by adjusting cable lengths.

5. Trigger Level Setting Error

a. In time interval:

$$\text{Setting Error} = \frac{\pm \text{ Trigger Level Accuracy}}{\text{Input Slew Rate at Start Trigger Point}} \quad \frac{\pm \text{ Trigger Level Accuracy}}{\text{Input Slew Rate at Stop Trigger Point}}$$

Table 1.1 - 1994 Specifications (Cont'd)

b. In rise/fall and pulse width:

$$\text{Setting Error} = \frac{\pm 60\ \text{mV}}{\text{Input Slew Rate at Trigger Point}}$$

6. Timebase Error

The fractional deviation of the timebase frequency from 10 MHz due to aging, temperature, voltage variations, etc. (See oscillator specifications for details.)

SECTION 2 INSTALLATION

2.1 INTRODUCTION

2.1.1 This section describes the unpacking and inspection, reshipment, rack installation; miscellaneous option installation, power connections, and storage/temperature requirements for the 1994.

2.2 UNPACKING AND INSPECTION

2.2.1 Before unpacking the counter, check the exterior of the shipping carton for any signs of damage. All irregularities should be noted on the shipping bill. Remove the instrument carefully from its carton, preserving the factory packaging as much as possible. Inspect the counter for any defect or damage. Notify the carrier immediately if any damage is apparent. Have a qualified person check the instrument for safety before use.

2.3 RESHIPMENT INSTRUCTIONS

2.3.1 Use the original packaging if it is necessary to return the counter to Racal-Dana for calibration and/or servicing. The original shipping carton and the instrument's plastic-foam form will provide the necessary support for safe reshipment. If the original packaging is unavailable, reconstruct it as much as possible. Wrap the counter in plastic; then use plastic spray foam to surround and protect the instrument. Reship in either the original or new, sturdy shipping carton.

2.4 BENCH OPERATION

2.4.1 The 1994 is equipped with a tilt-bail to elevate the front of the instrument for easy operation. The tilt-bail is attached to the two front feet on the bottom of the counter. For use, the bail is pulled down to its vertical position.

2.5 EQUIPMENT RACK INSTALLATION

2.5.1 The 1994 can be mounted in a standard 19-inch equipment rack using either the Fixed-Mount Option 60 or Slide-Mount Option 65. Installation instructions for these two options follow.

2.5.2 Fixed-Mount Option 60 Installation

2.5.2.1 Refer to Figure 2.1 for this procedure. The installation package includes:

a. Flange-Mount angle-brackets (2)

b. Front corner-inserts for non-handle installations (2)

c. Flathead #8-32 x 1/2 screws (4)

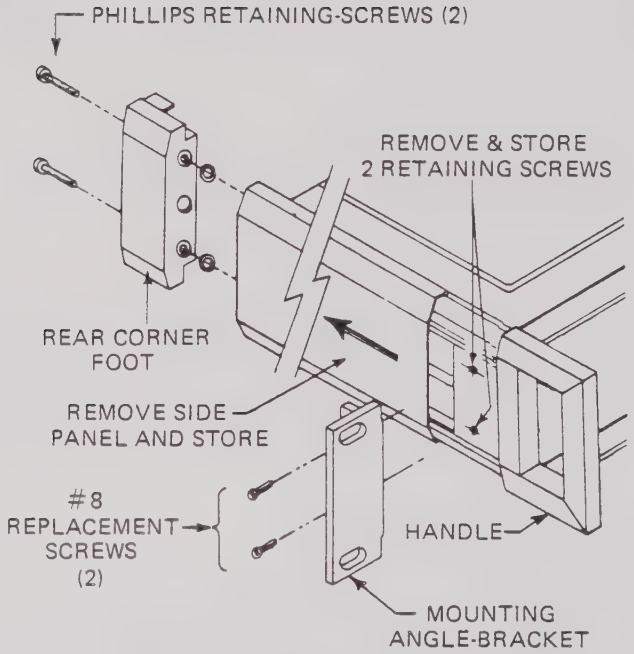


Figure 2.1 - Fixed-Mount Angle-Bracket Detail

2.5.2.2 Remove the tilt-bail by applying pressure inward on the bail legs, then unhooking the bail from the bench feet.

2.5.2.3 Remove the bench feet and side panels by completing the following steps:

a. Unscrew the two phillips head screws from each rear corner-foot. This frees the corner-feet, covers, and side panels

b. Remove the two rear corner-feet from the case

c. Place the instrument bottom-up, then slide the bottom cover 1/2 inch towards the rear panel and lift off. The top cover slides off in the same manner

d. Remove the four bench feet from the bottom cover by unscrewing the phillips head retaining screws from each foot

e. Slide the side panels down their retaining tracks towards the rear, then remove the panels. (With side panels off, the retaining screws-2 per side-for the front handles/corner inserts are exposed.)

2.5.2.4 Install the flange-mount angle-brackets by completing the following steps:

a. Remove the retaining screws for both handles/corner inserts, leaving the handles/corner inserts in place

b. Place an angle bracket over each handle/corner insert, aligning the mounting holes over the retaining screw holes

c. Insert two replacement flathead #8-32 x 1/2 screws through each angle bracket and handle/corner-insert combination, then screw securely to the case

2.5.2.5 Reassemble the instrument by replacing the top and bottom covers into the groove in the front panel. Do not attempt to replace the instrument's side panels. Complete the procedure by screwing the two rear corner-feet to the case.

2.5.2.6 Store the following items in a convenient location:

Two side-panels, four bench feet and retaining screws, and four replaced retaining screws from the front handles/corner inserts

2.5.3 Slide-Mount Option 65 Installation

2.5.3.1 Refer to Figures 2.2-2.6 for this procedure. The installation package includes:

a. Front corner-inserts for nonhandle installations (2)

b. Flange-Mount angle-brackets (2)

c. Alignment blocks (6)

d. Front rack-brackets (2) } interchangeable

e. Rear rack-brackets (2) }

f. Triple-rail slide-mount assemblies (2)

g. Self-Anchoring #10-32 tinnerman nuts (12)

h. Phillips panhead #10-32 x 1/2 screws (8)

i. Slotted panhead #8-32 x 3/8 screws with nuts, washers, and lock washers (6 each)

j. Phillips panhead self-tapping #8-32 x 5/16 screws (8)

k. Phillips flathead #8-32 x 1/2 screws (4)

l. Phillips panhead #10-32 x 3/4 screws (4)

m. Alignment #8 x 1/16 (spacers) washers (2)

n. Cover retaining-brackets (2)

2.5.3.2 Prepare the instrument for installing the alignment blocks in the side channels of the unit. Refer to Figures 2.1 and 2.2 and complete the following steps:

a. Remove the two rear corner-feet by extracting the two phillips retaining screws from each foot

b. Slide the top and bottom covers 1/2 inch towards the rear panel, then lift them off

c. Remove the four bench feet and tilt-bail from the bottom cover

d. Slide the side panels down their retaining tracks towards the rear, then remove the panels

e. Store the four panels, four bench feet, and tilt-bail in a convenient location

f. Remove the two front handles/corner inserts from the frame by extracting the two retaining screws from each handle or corner insert

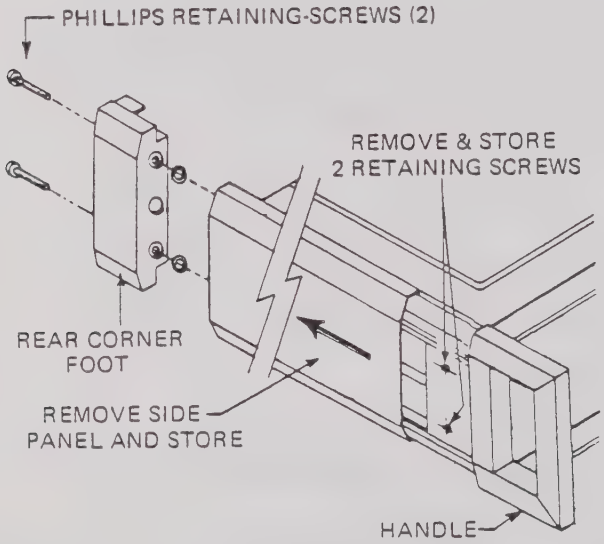


Figure 2.2 - Rear Corner Foot, Side Panel, and Handle Detail

2.5.3.3 Refer to Figure 2.3 for alignment block loading. Slide the alignment blocks down the center channel of the frame on each side of the instrument. Three alignment blocks per side should be loaded for full-rack depth units; two blocks for intermediate-rack depth units. The two screw holes in each alignment block should be at center position and below, relative to the center channel.

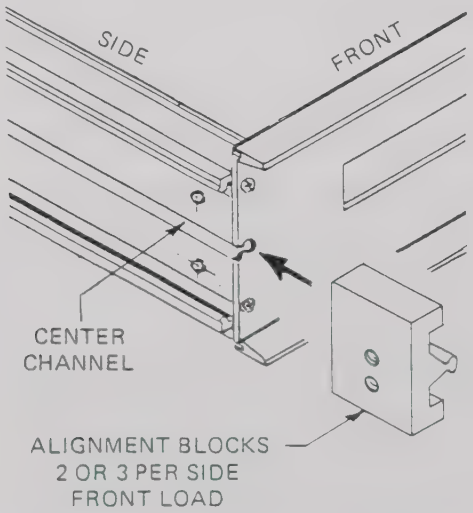


Figure 2.3-Loading the Alignment Blocks

2.5.3.4 Replace the top and bottom covers on the instrument. Fasten the covers using the two cover retaining-brackets (see Figure 2.6) and four phillips panhead screws (two per side) originally removed from the rear corner-feet. The instrument is now ready for attachment of the two triple-rail slide-mount assemblies.

2.5.3.5 Refer to Figure 2.4A/B. Prepare the triple-rail slide-mount assembly for equipment rack installation. First, note that the instrument-rail and rack-rail holes are accessible either directly or through the enlarged holes in the center-rail (as the assembly is extended or retracted). Complete the following procedure:

a. Place a front rack-bracket on the workbench, slotted flange facing down

b. Position the front end (i.e., slide-out end) of the slide-mount assembly over and parallel to the front rack-bracket. The rack-rail should rest within the bracket, about 3/4 inch from the bracket's front edges

c. Adjust the rails, aligning the front rack-rail hole with the center-rail access hole and mounting slot in the front rack-bracket. Insert a slotted panhead #8-32 x 3/8 screw through the holes. Attach a washer, lock washer, and nut to the screw and secure firmly, maintaining the 3/4-inch dimension to the front of the bracket

NOTE:

Measure the distance between the front and rear mounting-rails of the rack at this point. If the distance is **less** than 20 inches, follow instruction "d" next; if the distance is **greater** than 20 inches, follow instruction "e".

d. Fully extend the slide-mount assembly. Position of a rear-bracket (with two elongated mounting slots) on the rear of the assembly in the same way as the front rack-bracket. Align the mounting slot closest to the slotted flange with the rear rack-rail hole. Insert a slotted panhead #8-32 x 3/8 screw through the holes. Attach a washer, lock washer, and nut to the screw and secure the rear rack-bracket loosely to the slide-mount assembly

e. Fully extend the slide-mount assembly. Position a rear rack-bracket on the rear of the assembly in the same way as the front rack-bracket. Align the mounting slot with the rear rack-rail nail hole. Insert a slotted panhead #8-32 x 3/8 screw through the holes. Attach a washer, lock washer, and nut to the screw and secure the rear rack-bracket loosely to the slide-mount assembly

f. Complete the other slide-mount and rack-bracket assembly in the same manner as just described

g. Slide two self-anchoring #10-32 tinnerman nuts on the front and rear rack-brackets at the top and bottom slots of both slide-mount assemblies

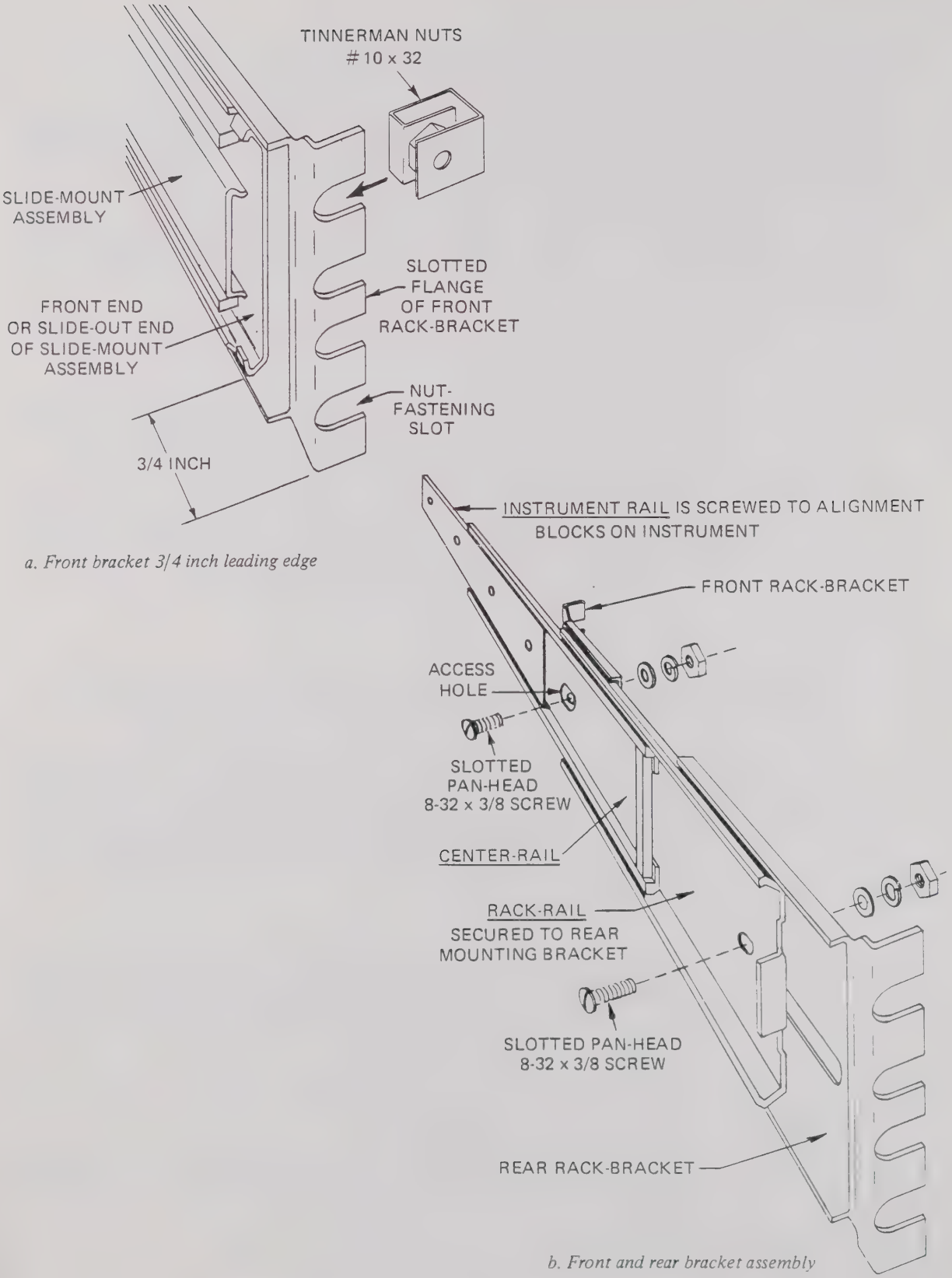

TINNERMAN NUTS
#10 x 32
SLIDE-MOUNT ASSEMBLY
SLOTTED FLANGE OF FRONT RACK-BRACKET
FRONT END OR SLIDE-OUT END OF SLIDE-MOUNT ASSEMBLY
NUT-FASTENING SLOT
3/4 INCH
a. Front bracket 3/4 inch leading edge
INSTRUMENT RAIL IS SCREWED TO ALIGNMENT BLOCKS ON INSTRUMENT
FRONT RACK-BRACKET
ACCESS HOLE
SLOTTED PAN-HEAD 8-32 x 3/8 SCREW
CENTER-RAIL
RACK-RAIL SECURED TO REAR MOUNTING BRACKET
SLOTTED PAN-HEAD 8-32 x 3/8 SCREW
REAR RACK-BRACKET
b. Front and rear bracket assembly

Figure 2.4A/B–Slide–Mount and Bracket Assembly

2.5.3.6 The assistance of a second person will be needed for the following instrument-rack assembly. Secure the slide-mount assembly in the designated area of the instrument rack using the procedure below.

NOTE:

If the mounting-rail of the instrument rack is tapped for #10-32 screws, drill out two places for each bracket using a 1/4 inch diameter bit. Proceed with the assembly:

a. Hold the front end of the slide-mount assembly behind the front mounting-rail of the rack, while the second person holds the rear end of the assembly

b. Secure the front rack-bracket to the front mounting-rail using two phillips panhead #10-32 x 1/2 screws. Seat the front rack-bracket firmly against the mounting-rail before tightening these screws

c. Install the other front rack-bracket on the front mounting-rail in the same manner

d. Set the front dimension between the two slide-mount assemblies at 16 5/8 inches

e. Adjust the length of the rear rack-brackets to touch the inside of the rear mounting-rail. Tighten the rear rack-bracket assembly screws

f. The distance between the two slide-mount assemblies at the rear-bracket should be 16 5/8 inches. Should a filler plate be required to secure the slide-mount assembly to the rear rack mounting-rail at 16 5/8 inches, use the dimensions given in Figure 2.5 to determine filler-plate size

NOTE:

The rear rack-bracket may require adjustment to accommodate the thickness of the filler plate.

g. Secure the rear rack-bracket mounting-rail (or filler plate) using two phillips panhead #10-32 x 1/2 screws in each bracket

h. The triple-rail slide-mount assemblies should move freely to their maximum extended positions. If not, remove any obstacle before installing the instrument

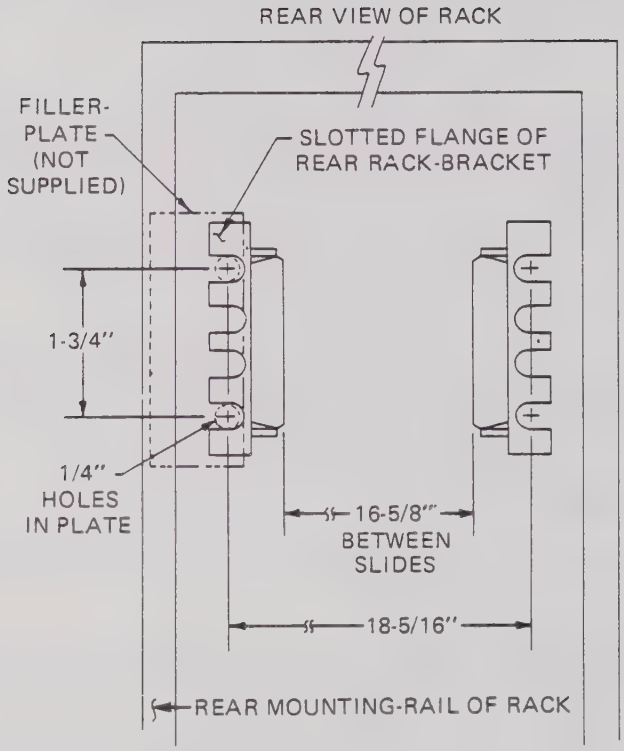


Figure 2.5 - Rear End Slide-Mount Rack Dimensions

2.5.3.7 Refer to Figure 2.6 (with inset). The assistance of a second person will be needed for the following slide-mount assembly-to-instrument installation.

a. Extend the rails of the slide-mount assemblies to their maximum position. Insert a phillips panhead self-tapping #8-32 x 5/16 screw inward through the first mounting hole in the instrument rail. Place an alignment (spacer) washer on the screw on the other side of the instrument-rail

b. Screw the flange-mount angle-bracket to pull-up position on the instrument-rail. Check that the alignment washer remains between the angle bracket and instrument-rail. Repeat this procedure for the other instrument-rail

NOTE:

For 5-1/4 inch high instruments, use the **bottom** hole of the angle bracket in step "b" above.

c. With the help of a second person, position the instrument between the fully extended rails. For full-depth instruments, the rear alignment-block hole should be situated immediately behind the fourth attachment hole in the center-rail. For immediate-depth instruments, the rear alignment-block hole should be located behind the third attachment hole

NOTE:

For 3-1/2 inch high instruments, position the rail access hole over the **top** alignment-block hole; for 5-1/4 inch high instruments, use the **bottom** hole.

d. Insert a phillips panhead self-tapping #8-32 x 5/16 screw through the rail access hole and screw it to pull-up position in the alignment block. At the same time, position the flange-mount angle-bracket in its approximate final location in the side frame channels. Align the other alignment-block screw holes with their attachment holes in the instrument-rail. Insert phillips panhead self-tapping #8-32 x 5/16 screws in the alignment blocks and fasten to pull-up position. Repeat this procedure for the other rail

e. Slide the handle/corner insert between the side frames and each angle bracket

f. Align the handle/corner insert and angle-bracket holes with their retaining screw holes in the side frame

g. Insert two phillips flathead #8-32 x 1/2 screws through the handle/corner insert and angle-bracket combinations, then fasten firmly to the frame

h. Securely fasten all self-tapping screws in the instrument-rail. The instrument should slide freely on the rails

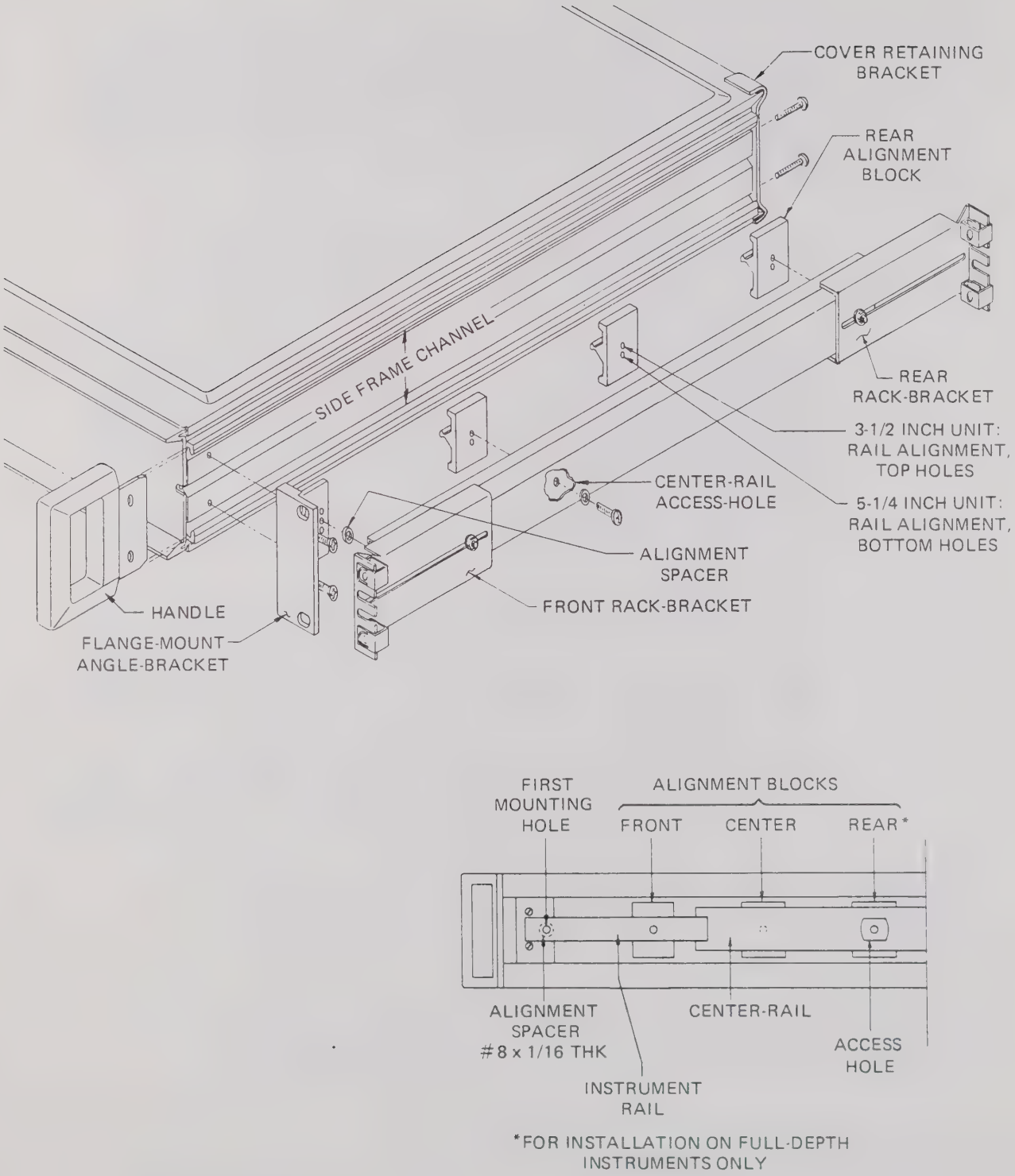


Figure 2.6-Slide-Mount and Instrument Assembly (with inset)

2.5.3.8 The following assembly is required to lock the instrument into its normal operating position on the rack:

a. Slide two self-anchoring #10-32 tinnerman nuts on the mounting-rail of the rack (each side). These nuts should be aligned with the angle-bracket slots. Omit the tinnerman nuts if the mounting-rail is tapped for #10-32 screws

b. Slide the instrument fully into the rack until the angle brackets strike the slide-mount bracket screws. Secure the instrument in place using four phillips panhead #10-32 x 3/4 screws

2.6 MISCELLANEOUS OPTION INSTALLATION

2.6.1 Ovened Frequency Standards 404392 and 404384 (Options 04A and 04E)

2.6.1.1 Refer to Figure 2.7 for these procedures. The installation package includes:

a.	Oscillator assembly (1)	P/N 404397 for Option 04A P/N 404386 for Option 04E
b.	#4 split lock washers (2)	P/N 617127
c.	#4 flat washers (2)	P/N 617102
d.	M3 x 8 screws (2)	P/N 611067

2.6.1.2 Installation

a. Disconnect the AC power cord at the rear panel

b. Loosen, but don't remove, the two rear corner-feet by unfastening the four retaining screws (two per foot). Back the corner feet out approximately 5/8 inch. Slide the top cover toward the rear of the unit, then lift up and out to remove

c. Remove the currently fitted frequency standard, according to the following instructions:

<u>If the standard 10 MHz oscillator is installed</u>:

1. Remove the two screws and washers attaching the oscillator assembly to the rear panel via the two threaded standoffs

2. Disconnect the flying lead from the motherboard at SK14, then lift the oscillator assemby out of the chassis

<u>If Option 04A/04E is installed</u>:

1. Remove the two screws and washers attaching the oscillator assembly directly to the rear panel

2. Disconnect the flying lead from the motherboard at SK14, then lift the oscillator assembly out of the chassis

d. Connect the flying lead of the new oscillator assembly to SK14 on the motherboard

e. Secure the oscillator assembly to the rear panel using the two M3 x 6 screws and two #4 lock washers. For Option 04A/04E, the screws pass directly into the top of the oscillator assembly; for the standard oscillator, the screws fasten the oscillator to the rear panel via two threaded standoffs

f. Replace the top cover; firmly secure the two rear corner-feet, completing the installation

2.6.2 Frequency Standard Multiplier 404399 (Option 10)

2.6.2.1 Refer to Figure 2.7 for this procedure. The installation package includes:

a.	Frequency multiplier PCB (1)	P/N 19-1164
b.	#4 split lock washers (2)	P/N 617127
c.	#4 flat washers (2)	P/N 617102
d.	M3 x 8 screws (2)	P/N 611067

2.6.2.2 Installation

a. Disconnect the AC power cord at the rear panel

b. Loosen, but don't remove, the two rear corner-feet by unfastening the four retaining screws (two per foot). Back the corner feet out approximately 5/8 inch. Slide the top cover toward the rear of the unit, then lift up and out to remove

c. If an ovened frequency standard (Option 04A/04E) is installed, remove it according to paragraph 2.6.1.2

d. Remove the 2-pin shorting link at SK16. Connect the frequency multiplier PCB to the motherboard at SK16 and SK17, with the threaded spacers toward the adjacent shield (as shown)

e. Secure the option PCB to the shield using the two M3 x 6 screws and two #4 split lock washers

f. If removed, replace and secure the ovened frequency standard removed in step (c)

g. Replace the top cover; firmly secure the two rear corner-feet, completing the installation

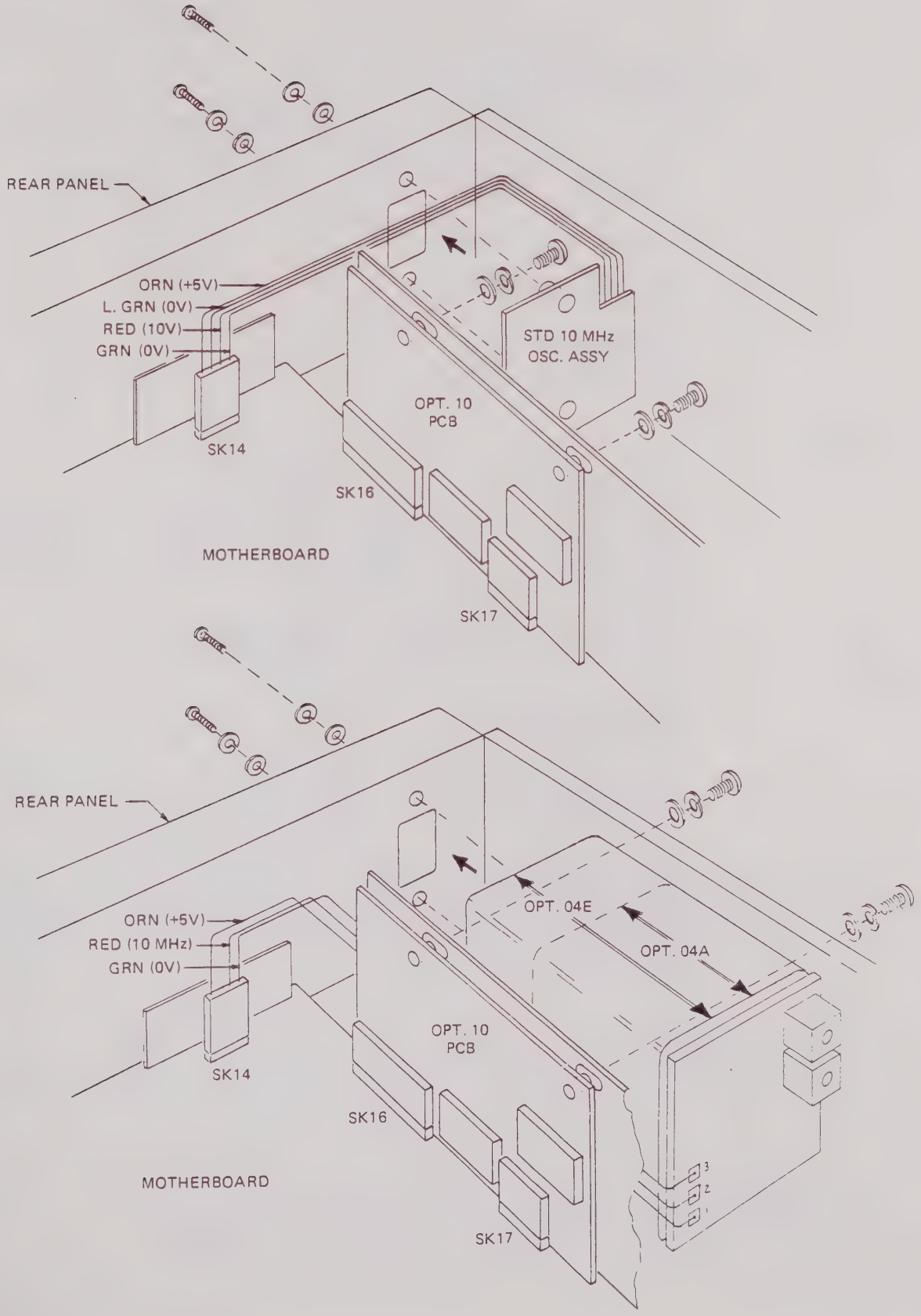


Figure 2.7 - Options 04A/04E and 10 Installation

2.6.3 1.3 GHz Input C 404398 (Option 41)

2.6.3.1 Refer to Figure 2.8 for this procedure. The installation package includes:

a. Input C (1.3 GHz) PCB including coaxial cable with snap-on BNC connector (1) P/N 19-1142-S-125

b. Fused BNC connector (1) P/N 601235

c. #4 split lock washers (2) P/N 617127

d. #4 flat washers (2) P/N 617102

e. M3 x 8 screws (2) P/N 617067

2.6.3.2 Installation

a. Disconnect the AC power cord at the rear panel

b. Loosen, but don't remove, the two rear corner-feet by unfastening the four retaining screws (two per foot). Back the corner feet out approximately 5/8 inch. Slide the top cover toward the rear of the unit, then lift up and out to remove

c. Connect the Input C PCB to the motherboard at PL7 with the two threaded spacers toward the right-hand side frame

d. Secure the option PCB to the shield, using the two M3 x 6 screws and two #4 split lock washers

e. Remove the black front-hole plug from INPUT C and screw the fused BNC connector into the front panel. Store the front-hole plug in a convenient place

f. Connect the coaxial cable from the option PCB to INPUT C (as shown) using the snap-on BNC connector

g. Replace the top cover; firmly secure the two rear corner-feet, completing the installation

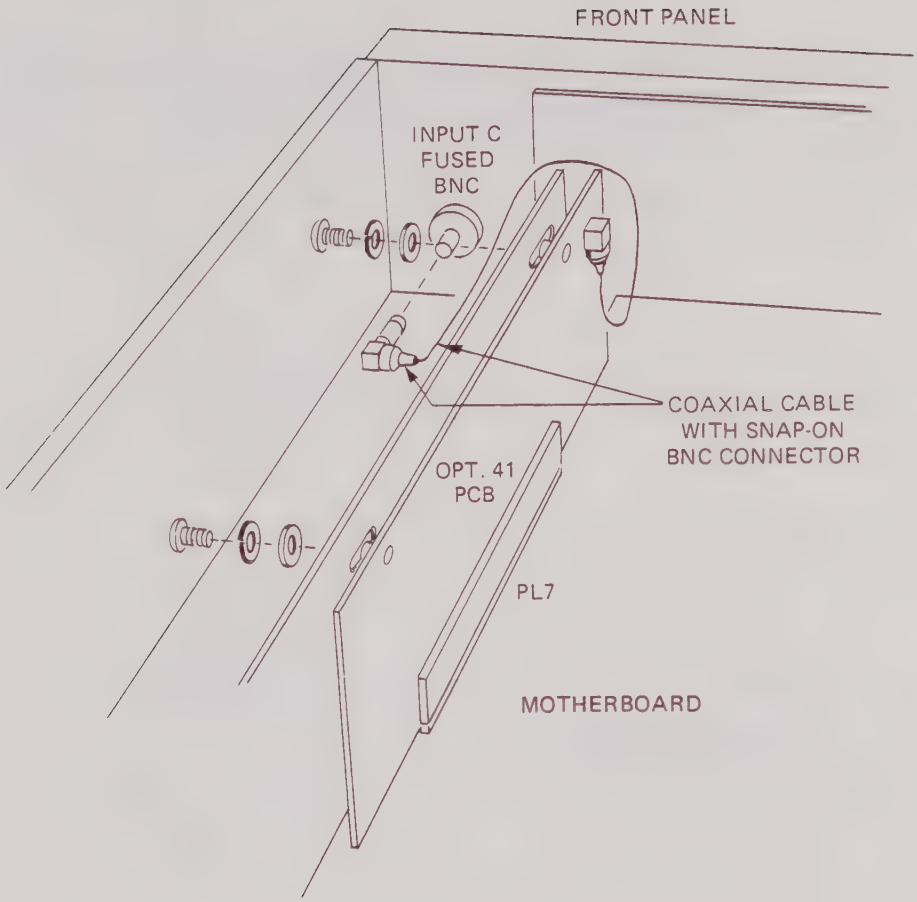


Figure 2.8 - Option 41 Installation

2.7 POWER CONNECTIONS

2.7.1 Before operating the counter, verify that the AC voltage selector is correctly set for the local AC supply. The counter operates on 100, 120, 220, or 240 volts, 45 to 450 Hz. The present voltage range can be viewed through the small window on the rear panel between the power cord socket and the line fuse (see Figures 2.9 and 3.2).

2.7.2 Line Voltage Selection

2.7.2.1 The line voltage setting is easily changed by repositioning the small voltage selector card, which is inserted vertically in its slot close to the rear panel. Refer to Figure 2.9 and use the following procedure:

a. Remove the power cord from its socket

b. Loosen, but don't remove, the two rear corner-feet by unscrewing the two phillips retaining screws from each foot. Back the corner feet out approximately 5/8 inch. Slide the top cover 1/2 inch towards the rear panel, the lift the former off

c. Extract the voltage selector card by firmly pulling it upwards until it is disengaged from its socket. Reinsert the card so that the desired setting is visible in the rear-panel window

d. Slide the top cover back into place and resecure the two rear corner feet

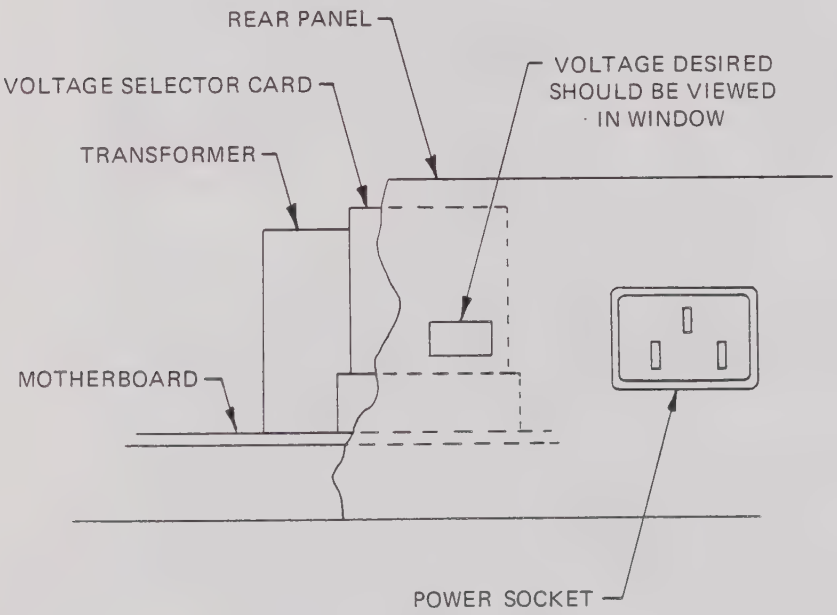


Figure 2.9 - AC Line Voltage Selection

2.7.3 Power Cord and Grounding

2.7.3.1 The front panel and instrument case are grounded in accord with MIL-T-28800C, protecting the user from possible injury due to shorted circuits.

NOTE:

The counter is designed to meet IEC Publication 348, "Safety Requirements for Electronic Apparatus for Class I Instruments".

2.7.3.2 A protective ground terminal, forming part of the rear-panel input socket, is provided. The counter is supplied with a detachable 3-core power cord. Only this cord should be used.

2.7.3.3 Use only AC power outlets having a protective ground for connection to the counter. **DO NOT USE** 2-core extension cords or 3-prong to 2-prong adapters that don't provide a protective ground connection. Connection of the power cord to the power outlet must be made in accordance with the following standard color code:

	American	European
Live	Black	Brown
Neutral	White	Blue
Ground (Earth)	Green	Green/Yellow

2.7.3.4 Also, all devices connected to or in proximity with the 1994 must maintain the third-wire ground (earth) intact as set forth in current regulations.

2.7.4 Line Fuse

2.7.4.1 Check that the rating of the line fuse is suitable for the AC voltage range in use. The fuse should be a 1/4 in. x 1 1/4 in., glass cartridge, Slow-Blow type. Line voltage settings of 100 or 120V should have a 0.5A Slow-Blow fuse installed; settings of 220 or 240V should have a 0.25A Slow-Blow fuse installed.

2.8 STORAGE AND TEMPERATURE

2.8.1 The 1994 can be stored at temperatures ranging from -40°C to +70°C at 75% relative humidity without adverse effects to PCBs or components. The counter must be brought within its specified operating range of 0°C to +50°C before power-on.

2.9 FUNCTIONAL CHECK

2.9.1 Introduction

2.9.1.1 The following test procedure confirms whether or not the 1994 is performing correctly by checking most of the counter's circuitry. The procedure should be conducted when the 1994 is first put into service and after shipment to a new location.

2.9.1.2 Now perform the following procedure:

a. Connect the 1994 to a suitable AC power supply

b. Power-on the counter. Verify that the instrument type number "1994" is displayed for about two seconds, followed by the software issue number

NOTE:

Home-state conditions for the 1994 are listed in Subsection 3.2.3. Consult as required.

c. Press the FUNCTION ↑ key once; the CHECK LED should light. Verify that the display shows 10.0000000 E6 and that the GATE LED flashes

d. Press the RESOLUTION ↓ key five times, verifying that the display resolution decrements by one digit each key press

e. Press the RESOLUTION ↑ key to increase the resolution to nine display digits

2.9.1.3 As required, the following additional tests may be performed using the 1994's special functions. Make sure the 1994 is in the Check mode before executing these tests.

a. Press key sequence <71> SHIFT STORE SF SHIFT SF. Verify that all LEDs, except those for TRIG A, TRIG B, GATE, and STBY, flash on and off every two seconds.

b. Press key sequence SHIFT SF. Verify that SF LED is not lit

c. Provide a 50Ω coaxial test lead fitted with BNC connectors. The lead should be 60 cm to 1m long.

d. Using the coaxial test lead, connect the 10 MHz STD. OUTPUT BNC (see Figure 3.2) on the rear panel to the front-panel Input A connector

e. Press key sequence <77> SHIFT STORE SF SHIFT SF. This test verifies the proper operation of Input A's input relays. Confirm that the display shows *0.******* 0 Hz where * is a blanked digit. The X10, 50Ω, DC, FILTER, and COM A LEDs for Input A should light in turn

f. Disconnect the coaxial lead from Input A. The display should show an error number after a few seconds. See Table 3.14 for error codes

g. Press key sequence SHIFT SF. Verify that SF LED is not lit

h. Using the same test lead, connect the 10 MHz STD. OUTPUT BNC to the front-panel Input B connector

i. Press key sequence <78> SHIFT STORE SF SHIFT SF. This test verifies the proper operation of Input B's input relays. Confirm that the display shows *0.******* 0 Hz as in step d. The X10, 50Ω, and DC LEDs for Input B should light in turn

j. Disconnect the coaxial lead from Input B and the 10 MHz STD. OUTPUT BNC. The display should show Er 56

k. Press key sequence SHIFT SF. Verify that SF LED is not lit

l. Turn the 1994 off

SECTION 3 LOCAL OPERATION

3.1 INTRODUCTION

3.1.1 This section contains information for operating the 1994 as a bench instrument. It provides General Operating Information, Front and Rear Panel Descriptions, and Operating Procedures.

3.2 GENERAL OPERATING INFORMATION

3.2.1 If the counter is being used for the first time or at a new location, ensure that the voltage selector is set for the correct local AC supply before turning on the instrument. Refer to Subsection 2.7.2, as required, for details on line voltage selection.

3.2.2 Power-On and Self Test

3.2.2.1 Depress the POWER-ON/OFF button to its ON (▬) position. Power should now be supplied to the entire counter.

3.2.2.2 After a brief self-test, the counter will display the instrument number (1994) for approximately two seconds followed by the software issue number.

3.2.3 Home State

3.2.3.1 After self-test, the counter reverts to a home state, ready for operation. The following home-state conditions are selected after "self-test":

a. Manual Trigger levels A and B (0.00V): enabled

b. Time Interval DELAY: set at 200 μs (min. value)
(Verify using key sequence SHIFT RECALL DELAY)

c. GATE Time: 100 ms
(Verify using key sequence SHIFT RECALL GATE)

d. Math constants X, Y, and Z: 0, 1, 1, respectively

NOTE

The user may set math constant Z to zero. However, any attempt to use the math function with this value set will cause the generation of an error code.

e. FREQ A (8-digit resolution): enabled

f. Attenuation: 1X

g. Input Impedance: 1MΩ for Inputs A and B

h. Separate inputs (i.e., Common LED A is off)

i. Filter: off

j. Slopes A and B: positive

k. Special Functions disabled (none stored)

l. Input A and B trigger levels: zero, displayed levels are off

m. Hold: off

n. Resolution: on

o. Input coupling: AC for Inputs A and B

3.2.4 Main Display

3.2.4.1 Readings are displayed in engineering format with a 9-digit mantissa, 1-digit exponent, and floating decimal point. It is assumed that the reading is positive unless (1) the negative-sign LED to the left of the display is lit, or (2) a negative sign precedes the displayed mantissa. The largest display reading is 999.999999 with a +9 exponent; the smallest displayed reading is 1.00000000 with a -9 exponent.

3.2.4.2 See Subsections 3.4.3 and 3.4.4, and Table 3.13 for details of gate time and resolution. The selected function and resolution determine the number of digits displayed in the mantissa. In the frequency, period, frequency ratio, and check functions, 3 to 10 digits (9 plus overflow) can be selected. To change from 9 to 10 digits, the RESOLUTION (↑) key must be held down for approximately two seconds. Also, the gate time may be programmed in increments rounded to the nearest 25.6 µs using the range of 200 µs to 99.9 s. Stored gate times are immediately enabled. When the RESOLUTION (↑↓) keys are pressed, the counter is stepped up or down the closest decadic multiple of 1 ms.

3.2.4.3 LED indicators for units in Hz (hertz), S (seconds) and V (volts) are located to the right of the exponent display. Units for some functions are implied. For example, phase angle measurements are in degrees. Seven LEDs (O/F, REM, ADDR, SRQ, EXT ARM, EXT STD, and GATE) are situated immediately below the display (see Table 3.1).

3.2.5 Keyboard Organization

3.2.5.1 The front panel of the 1994 is arranged logically by function into color-coded keyboard/LED groups. Refer to the front-panel figures and Table 3.1 for location and description. Listed below (left to right) are the keyboard groups with their color coding indicated in parentheses.

a. General Operating (gray)

b. FUNCTION (yellow)

c. DATA ENTRY (brown)

d. INPUT A (blue)

e. INPUT B (blue)

f. INPUT C (blue)

3.3 PANEL DESCRIPTIONS

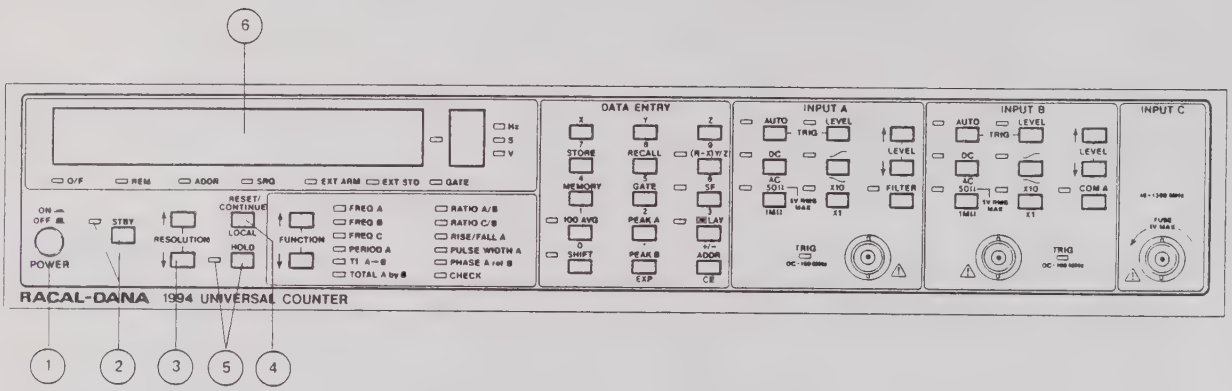
3.3.1 Front Panel Features

3.3.1.1 Refer to Table 3.1 and the front-panel figures. They show and describe front-panel controls, indicators, and connectors.

NOTE:

In the following table, LEDs shown in the "Item" column with an asterisk (*) are described in their lit condition. Certain LEDs are associated with toggle keys; their lit condition is specified.

Table 3.1 - Front Panel Controls, Indicators, and Connectors

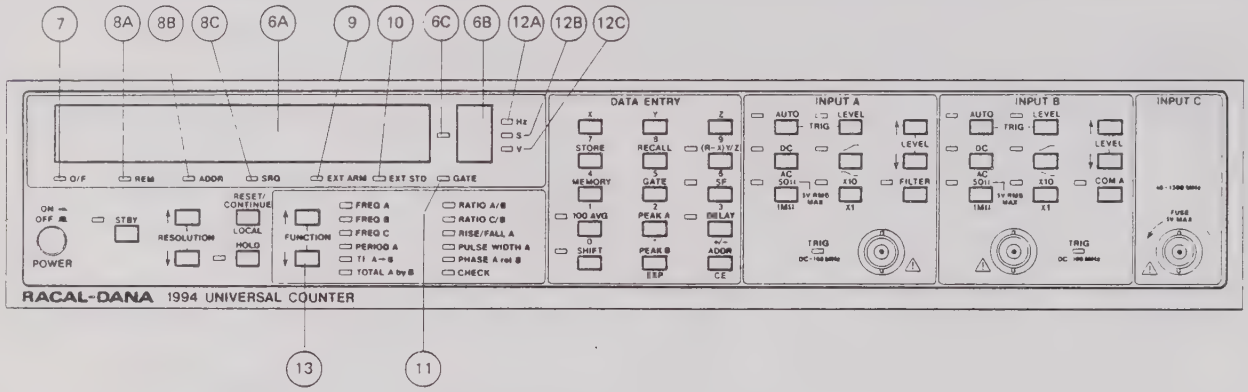


Reference	Item	Function/Description
1	POWER (ON/OFF) Button	Switches power ON or OFF. In ON position, power is supplied to the entire counter
2	STBY Key/LED	Toggles counter into and out of Standby. In Standby, power is supplied to the internal reference standard (timebase) and the LED is lit
3	RESOLUTION Keys (↑↓)	Select the number of display digits from 3 to 10 (9 with overflow). Use of these keys is function-dependent (see Sub-section 3.4.3). Each key press either steps the counter's resolution up (↑) or down (↓) by a decade. The up (↑) key must be held down for about two seconds to change from 9 to 10 display digits. When the RESOLUTION up (↑) and down (↓) keys are pressed, the gate time is disabled
4	RESET/CONTINUE, LOCAL Key	This key provides the following: **RESET** Terminates the measurement in progress, clears the display, and triggers a new measurement **NOTE:** In the HOLD mode, pressing this key triggers a new measurement cycle.

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
		CONTINUE Returns the counter to the measurement mode, triggers a new measurement cycle after the display of a recalled number or constant LOCAL Returns the counter to front-panel control from remote control on the GPIB, providing local lock-out has not been set
(5)	HOLD Key/LED	Toggles counter into and out of HOLD (single-shot measurement). LED lights in HOLD. In HOLD, the measurement in progress is completed and displayed. See NOTE under Reference (4). Special Function 61 causes the HOLD key to successively start and stop measurements for manual Totalize
(6)	Measurement Display	A 7-segment LED digital display. Uses engineering format with 9-digit mantissa, 1-digit exponent, and floating decimal point. The display shows one of the following depending on operational state: — measurement results — numbers for data entry — numbers for recall from constant or function stores, including trigger levels and peak values — error messages NOTE: The exponent LED is blanked and should be considered zero during the following: a. phase measurement b. totalize measurement with less than nine digits c. numeric entries not involving an exponent

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)

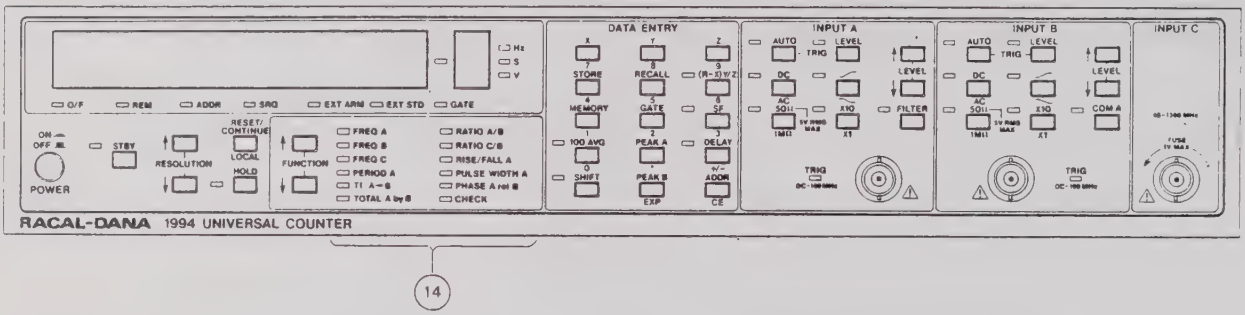


Reference	Item	Function/Description
6A	Mantissa Display LEDs*	Display 9-digit mantissa
6B	Exponent Display LED*	One-digit exponent number
6C	Exponent Sign LED*	Negative exponent
7	O/F LED*	Readout overflows the ninth digit of the display. With 10s or greater gate times, multiple overflows are possible
8	GPIB LEDs:	
8A	REM LED*	Counter under remote control over the GPIB interface
8B	ADDR LED*	Counter is being addressed as either a talker or listener over the GPIB interface
8C	SRQ LED*	Counter has transmitted a service request over the GPIB interface
9	EXT ARM LED*	External arming or gating (Special Functions 11-18) is controlling the measurement
10	EXT STD LED*	Counter is operating from an external frequency standard reference

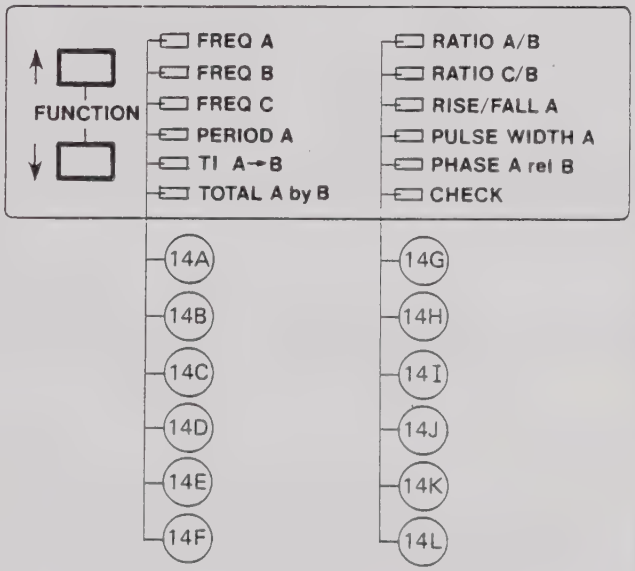
Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
		NOTE: Counter automatically switches to the external standard when the signal is applied
(11)	GATE LED*	Gate is open and a measurement is in progress
(12)	Display Unit LEDs:	NOTE: These LEDs do not light when a phase angle, ratio, totalize, math computation, or a constant is displayed
(12A)	Hz LED*	Units in Hertz for a frequency measurement
(12B)	S LED*	Units in Seconds for a time measurement
(12C)	V LED*	Units in Volts for voltage level
(13)	FUNCTION Keys (↑↓)	Select in succession the counter's measurement function. The corresponding FUNCTION LED is lit. Function selection "wraps around" at both ends

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)



Reference	Item	Function/Description
14	FUNCTION LEDs:	Indicate selected function

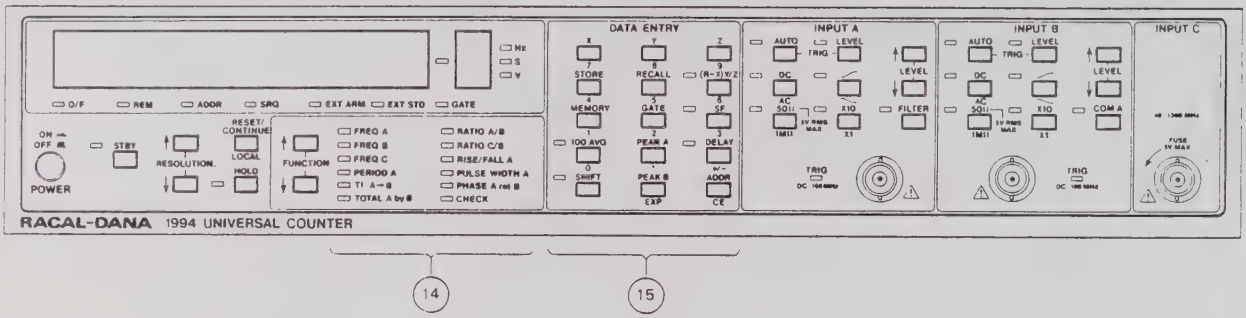


14A	FREQ A*	Input A Frequency-measures frequencies to 160 MHz (direct gating), providing a resolution of at least 9 digits in 1 s
14B	FREQ B*	Input B Frequency just as FREQ A except frequency measurement to 100 MHz

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
(14C)	FREQ C*	Input C Frequency (Option 41)-measures frequencies to 1.3 GHz with a resolution of at least 9 digits in 1 s at any frequency
(14D)	PERIOD A*	Input A Period-measures periods from 6.25 ns to 1.7 x 10^3/s, with up to 9-digits resolution per second of measurement
(14E)	TI A B*	Time Interval (Input A for start, Input B for stop). Intervals from -2 ns to 1 x 10^5/s can be measured. When in COM A mode, the measurement signal applied to Input A is directed to both Input A and B amplifiers
(14F)	TOTAL A by B*	Totalize (Input A events gated by Input B). Input A can totalize events at a rate up to 1 x 10^8/s. A positive slope selection on Input B starts positive, stops negative, and vice-versa
(14G)	RATIO A/B*	Ratio A/B (Ratio of Frequency A to Frequency B), with frequency range of DC to 100 MHz
(14H)	RATIO C/B*	Ratio C/B (Ratio of Frequency C to Frequency B)
(14I)	RISE/FALL A*	Selects Rise/Fall Time for Input A, depending on the trigger slope condition. Input A Rise Time (positive slope; 10% start and 90% stop trigger points). Input A Fall Time (negative slope; 90% start and 10% stop trigger points). Default state is Rise A. Changing either Input A or B trigger slope automatically changes the other input and sets the counter to Fall A. Minimum frequency is 50 Hz
(14J)	PULSE WIDTH A	Input A Pulse Width. Default state is Positive Pulse Width (positive start slope, negative stop slope, 50% trigger points). Changing either Input A or B trigger slope automatically changes the other input and sets the counter for Negative Pulse Width (negative start slope, positive stop slope, 50% trigger points). Minimum frequency is 50 Hz

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)



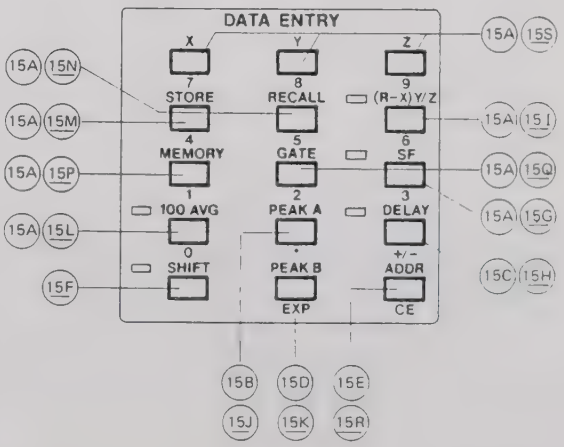
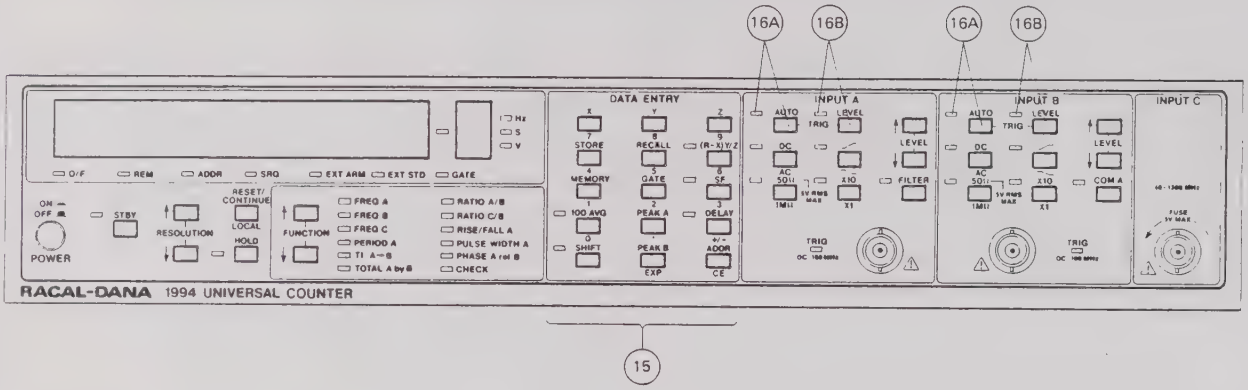
Reference	Item	Function/Description
14K	PHASE A rel B*	Phase difference (Input A relative to Input B) **NOTE:** Phase, Rise/Fall, and Pulse Width require a continuous signal during measurement
14L	CHECK*	Permits the 1994 to measure its own 10 MHz internal standard. The CHECK function can be expanded using special functions (See Subsection 3.4.10)
15	DATA ENTRY Keys/LEDs: **NOTE:** Designators for shifted key functions are underlined. Also, designator "150" is not used	Permit data entry and user interface with the 1994 other than input signal conditioning and measurement functions 

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
(15A)	Unshifted Key Functions: Numeric Keys (0-9)	Entry of numbers and constants for math, special functions, time-interval stop delays, trigger levels, and gate times. Also, used to recall machine setups. When a numeric key is pressed, the measurement in progress is aborted and the display shows the entered number
(15B)	Decimal Point (.) Key	Inserts decimal point during numeric entry
(15C)	Positive/Negative (+/-) Sign Key	Toggles sign of entered number (mantissa and/or exponent) between positive (no sign displayed) and negative (sign displayed)
(15D)	EXP Key	Changes the data entry mode so that the next number entered is the exponent
(15E)	CE Key	Clears current display and starts a new reading
(15F)	Shifted Key Functions: SHIFT Key/LED*	Enables any shifted key function. After pressing a shifted key function (except for STORE, RECALL, and MEMORY), counter immediately returns to its unshifted state with the SHIFT LED turning off. Does not clear the display
(15G)	SF Key/LED*	Enables all selected special functions (SHIFT SF). Also stores (<NN>SHIFT STORE SF) and recalls (SHIFT RECALL SF) special functions. See Subsection 3.4.10 for details
(15H)	DELAY Key/LED*	Enables a time-interval stop delay (SHIFT DELAY) in TI A→B and Totalize. Also, store (<value>SHIFT STORE DELAY) and recalls (SHIFT RECALL DELAY) a time-interval stop delay. Enabling a delay in a non-TI function produces an error message. Selecting a non-TI function when in delay disables DELAY and turns off the LED

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)

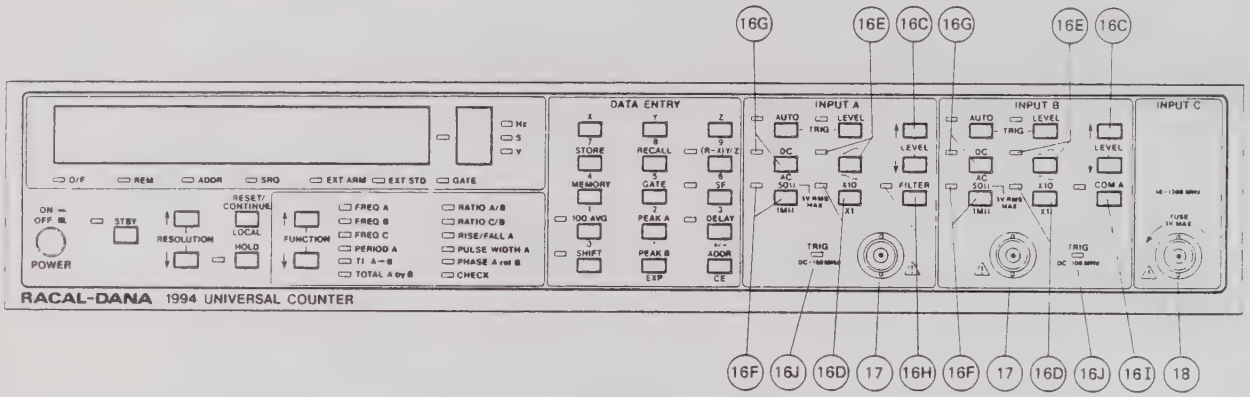


Reference	Item	Function/Description
15I	(R-X) Y/Z Math Key/LED*	Selection of Math Computation mode
15J	PEAK A Key	Displays positive and negative signal peaks of Input A by using key sequence SHIFT RECALL PEAK A
15K	PEAK B Key	Displays positive and negative signal peaks of Input B by using key sequence SHIFT RECALL PEAK B NOTE: During recall of PEAK A or B, the counter must be in the Auto-Trig mode
15L	100 AVE Key*	Permits counter to accumulate 100 gate measurements and display the average. A 1-decade improvement in resolution results. Enables the Average function using key sequence SHIFT 100 AVG, turning on the LED. Perform the same sequence again to disable the function and turn off the LED
15M	STORE Key	Stores constants for math functions, gate time, time-interval delay, and special functions. Used with MEMORY key to store complete measurement (i.e., machine) setups

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
(15N)	RECALL Key	Recalls constants for math functions, gate time, time-interval delay, special functions, and peak A and B levels. Used with MEMORY key to recall complete measurement (i.e., machine) setups
(15P)	MEMORY Key	Stores and recalls complete measurement setups (SHIFT STORE/RECALL MEMORY⟨N⟩ where ⟨N⟩ = 0 to 9). Attempted store or recall of an out-of-range setup number produces "Op Er" as error message
(15Q)	GATE Key	Stores and recalls gate time using corresponding key sequences ⟨value⟩ SHIFT STORE GATE or SHIFT RECALL GATE. The programmable gate time range is 200 µs to 99.9 s. Gate times are rounded off to the nearest 25.6 µs for display, but can be entered in any valid step size
(15R)	ADDR Key	Used to display the counter's GPIB address using key sequence SHIFT RECALL ADDR. See Subsection 4.3 for the address setting procedure
(15S)	X/Y/Z Keys	Store and recall of Math computation constants X, Y, and Z
(16)	INPUT A and B Keys/LEDs	Toggle the counter in and out of the Auto-Trig mode for Inputs A and B. The AUTO-TRIG LED lights in the Auto-Trig mode. Press the TRIG-LEVEL key to display the trigger level
(16A)	AUTO-TRIG Keys/LEDs*	
(16B)	TRIG-LEVEL Keys/LEDs*	Successive operations display Input A or B trigger levels or store the displayed trigger levels, returning the counter to its main function. The TRIG-LEVEL LED flashes when the trigger level is being displayed. The displayed trigger level can be changed using either the LEVEL ↑↓ keys or via the front panel keyboard.

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)



Reference	Item	Function/Description
(16C)	LEVEL ↑↓ Keys	Step the displayed trigger level for Inputs A and B either up (↑) or down (↓) in 20 mV increments. Use the key sequence TRIG-LEVEL LEVEL (↑↓) TRIG-LEVEL to store the displayed trigger level and return the counter to its main function
(16D)	Attenuation X10/X1 Keys/LEDs	Toggle Input A or B's attenuation between X1 and X10. The LED lights when X10 attenuation is selected. Changing the attenuation modifies the displayed trigger level by a factor of 10 (1.00V, X1; 10.0V, X10)
(16E)	⎍/⎏ Keys/LEDs	Toggle Input A or B's trigger slope between positive (⎍) and negative (⎏). LED lit in positive slope
(16F)	50Ω/1 MΩ Keys/LEDs	Toggle Input A or B's input impedance between 50Ω and 1 MΩ. LED lit in 50Ω mode
(16G)	DC/AC Keys/LEDs	Toggle Input A or B's coupling between DC and AC. LED lit in DC coupling
(16H)	FILTER Key/LED	Toggles a low-pass filter (50 kHz cutoff frequency) for Input A. LED lit when filter is on
(16I)	COM A Key/LED	Toggles Input A also to Input B. LED lit in COM A mode

Table 3.1 - Front Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
(16J)	TRIG LEDs/Inputs A and B	Tri-state LEDs indicating the counter's trigger status: a. LED Off-level too low b. LED Flashing-triggering c. LED On-level too high
(17)	INPUT(s) A and B	BNC connectors for INPUT(s) A and B. INPUT A (DC to 160 MHz) is used for all functions except Frequency C (Option 41). INPUT B (DC to 100 MHz) is used with INPUT A for Time Interval, Ratio A/B, Totalize, and Phase measurements. Input B is used with INPUT C for Ratio C/B. Special Function 21 internally exchanges INPUTs A and B (providing, e.g., PERIOD B, etc. measurement capability)
(18)	INPUT C (Option 41)	BNC connector for high-frequency INPUT C (40 MHz to 1.3 GHz range). INPUT C is used with INPUT B for Ratio C/B. Special Function 21 provides Ratio C/A capability. Protection against excessive signal levels (>5V rms) is provided by a fuse in the input socket

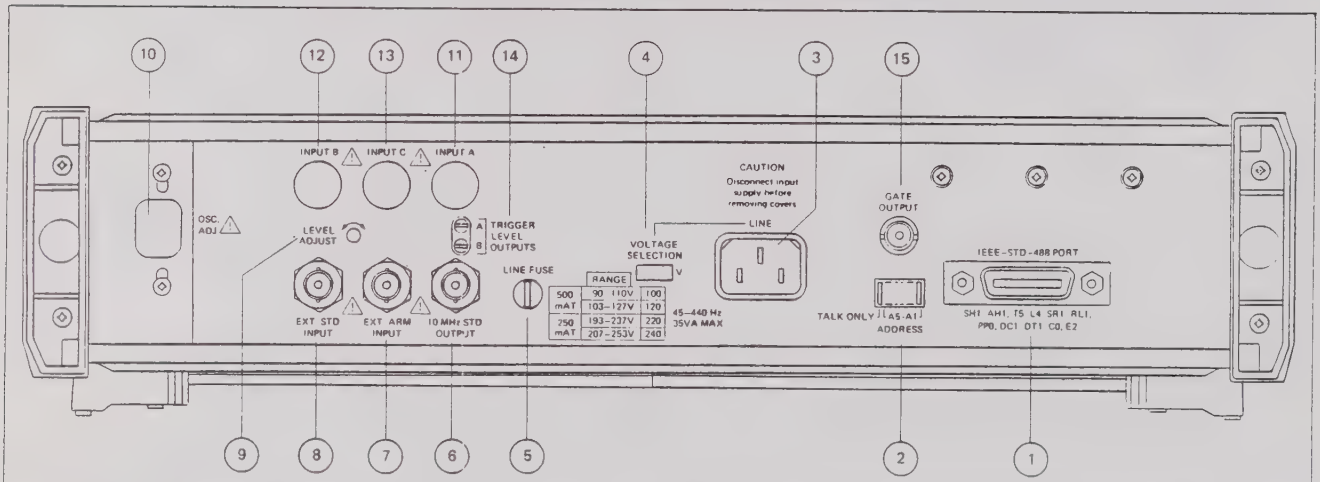
3.3.2 Rear Panel Features

3.3.2.1 Refer to Table 3.2 and the figure at top. They show and describe the rear panel controls and connectors.

NOTE:

Connectors (6), (7), (8), (10), (11), (12), and (14) are BNCs.

Table 3.2 - Rear-Panel Controls and Connectors



Reference	Item	Function/Description
(1)	GPIB Connector	GPIB (IEEE-STD-488-1978) connector
(2)	GPIB Address Switches	Switches A1 to A5 define the listen/talk addresses for the counter in the addressed mode. The Talk-Only switch should be in the "0" position. The counter is in the Talk-Only mode when the switch is set to "1"
(3)	AC Power Input Socket	Standard connector for the AC power supply
(4)	VOLTAGE SELECTION Window	Line voltage selection is changed by repositioning a small printed circuit card inside the counter. The selected voltage is viewed through the window
(5)	LINE FUSE	A 1/4 in. x 1-1/4 in. glass cartridge Slow-Blow fuse. Line fuse ratings for available line voltages are shown on the rear panel to the right of the fuse receptacle. See also Subsection 2.7.4 in this manual

Table 3.2 - Rear Panel Controls and Connectors (Cont'd)

Reference	Item	Function/Description
(6)	10 MHz STD. OUTPUT Connector	Output for 10 MHz internal reference signal
(7)	EXT. ARM INPUT Connector	Input for external arming/gating control signal
(8)	EXT. STD INPUT	Input for external reference frequency standard. The required frequency is 10 MHz, unless the reference frequency multiplier (Option 10) is installed. This option permits acceptance of 1 MHz, 2 MHz, 5 MHz as well as 10 MHz external reference signals
(9)	LEVEL ADJUST	Adjustment of the trigger level for the external arming input
(10)	OSC ADJ	Adjustment of the internal reference frequency standard
(11)	INPUT A Connector (Option 01)	Rear-panel Input A
(12)	INPUT B Connector (Option 01)	Rear-panel Input B
(13)	INPUT C Connector (Option 01 for units fitted with Option 41)	Rear-panel Input C
(14)	TRIGGER LEVEL OUTPUTS (A, B)	Outputs for Inputs A and B trigger levels. Voltage range at both pins is ±5.1V, regardless of attenuation
(15)	GATE OUTPUT	Output for negative-going TTL-compatible signal equivalent to the gate signal

3.4 OPERATING PROCEDURES

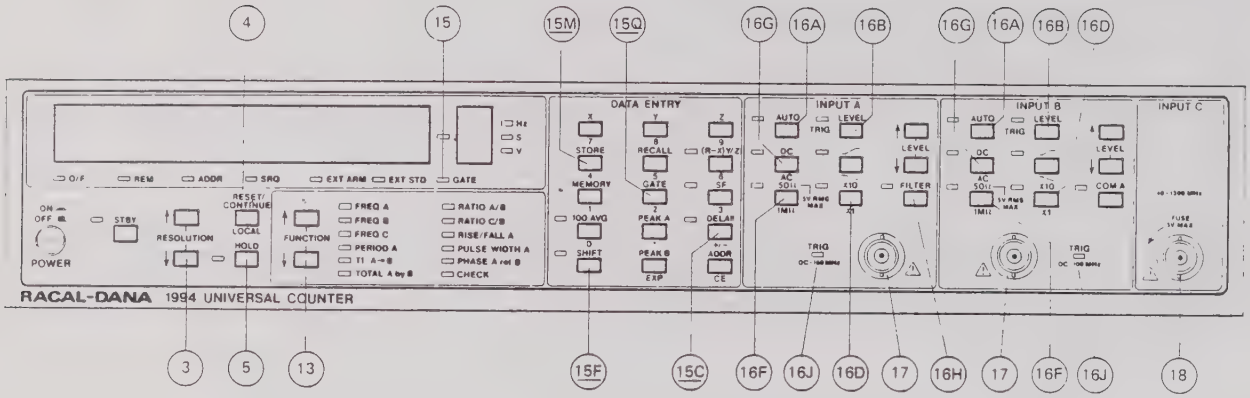
3.4.1 Measurement Functions

3.4.1.1 Tables 3.3 - 3.11 with figures describe the basic bench functions of the 1994.

NOTE:

Review as required Table 3.1, References 17 and 18, for use of Inputs A, B, and C, including Special Function 21 permitting interchange of Inputs A and B. See also Subsection 3.4.10 and Table 3.13 for special functions.

Table 3.3 - Frequency Measurement



1. Turn power on.

2. Select FREQ A, FREQ B, or FREQ C (Option 41) using FUNCTION keys (13).

3. If FREQ A or FREQ B is selected, set the AC/DC coupling (16G) and input impedance (16F) as required.

4. Select the X10 input attenuation (16D) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Connect the measurement signal to INPUT A (DC to 160 MHz) (17), INPUT B (DC to 100 MHz) (17), or INPUT C (40 MHz to 1.3 GHz) (18).

6. Select a specific gate time (valid range of 200 µs to 99.9 s) if desired. For small numbers, enter the gate time using the exponential format. The displayed gate time will be rounded to the nearest 25.6 µs. Use key sequence <value> SHIFT (15F) STORE (15M) GATE (15Q). Programmed gate times are immediately enabled with the resolution set accordingly. Skip step 7 if step 6 is being used to enter the gate time.

7. Use the RESOLUTION ↑↓ keys (3) to select the required display resolution and gate time if step 6 was not used (see Table 3.12).

8. If FREQ A or B is selected, either select AUTO-TRIG (A or B) (16A), or set the trigger level manually using key sequence TRIG-LEVEL (A or B) (16B) +/- (15C) <value> TRIG-LEVEL (A or B) (16B). Check that Input A/B TRIG LED (16J) flashes.

Table 3.3 - Frequency Measurement (Cont'd)

9. If a frequency below 50 kHz is to be measured in the presence of high frequency noise, select the FILTER (16H).

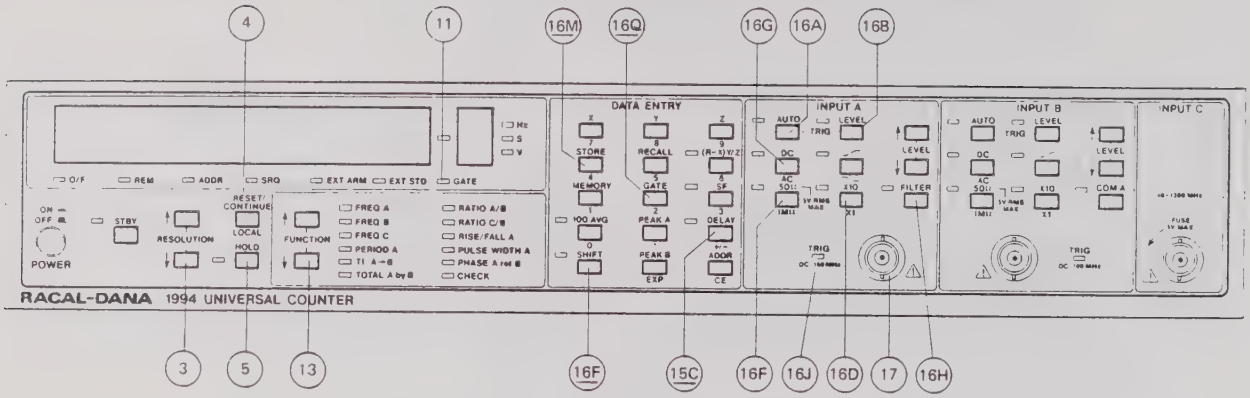
10. If external arming/gating is needed, connect the arming/gating signal and enter the required special function number. Enable special functions. Refer to Subsection 3.4.8 for special function numbers and procedures.

11. Select the HOLD mode (5) for single-shot measurements. Press the RESET (4) while in HOLD to trigger a new measurement.

12. If external arming/gating is in use, trigger a measurement cycle.

13. Ensure that the GATE LED (11) turns on during the measurement period.

Table 3.4 - Period Measurement



1. Turn power on.

2. Select PERIOD A using FUNCTION keys (13).

3. Set the AC/DC coupling (16G) and input impedance (16F) as required.

4. Select the X10 input attenuation (16D) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Connect the measurement signal to INPUT A (17). PERIOD B may be measured to 10 ns resolution using Special Function 21.

6. Select a specific gate time (valid range of 200 µs to 99.9 s) if desired. For small numbers, enter the gate time using the exponential format. The displayed gate time will be rounded to the nearest 25.6 µs. Use key sequence <value> SHIFT (16F) STORE (16M) GATE (16Q). Programmed gate times are immediately enabled with the resolution set accordingly. Skip step 7 if step 6 is being used to enter the gate time.

7. Use the RESOLUTION ↑↓ keys (3) to select the required display resolution and gate time if step 6 was not used (see Table 3.12).

8. Select AUTO-TRIG (16A), or set the trigger level manually using key sequence TRIG-LEVEL (16B) +/- (15C) <value> TRIG-LEVEL (16B). Check that Input A TRIG LEVEL LED (16J) flashes.

9. If a frequency below 50 kHz is to be measured in the presence of high frequency noise, select FILTER (16H).

10. If external arming/gating is needed, connect the arming/gating signal and enter the required special function number. Enable special functions. Refer to Subsection 3.4.8 for special function numbers and procedures.

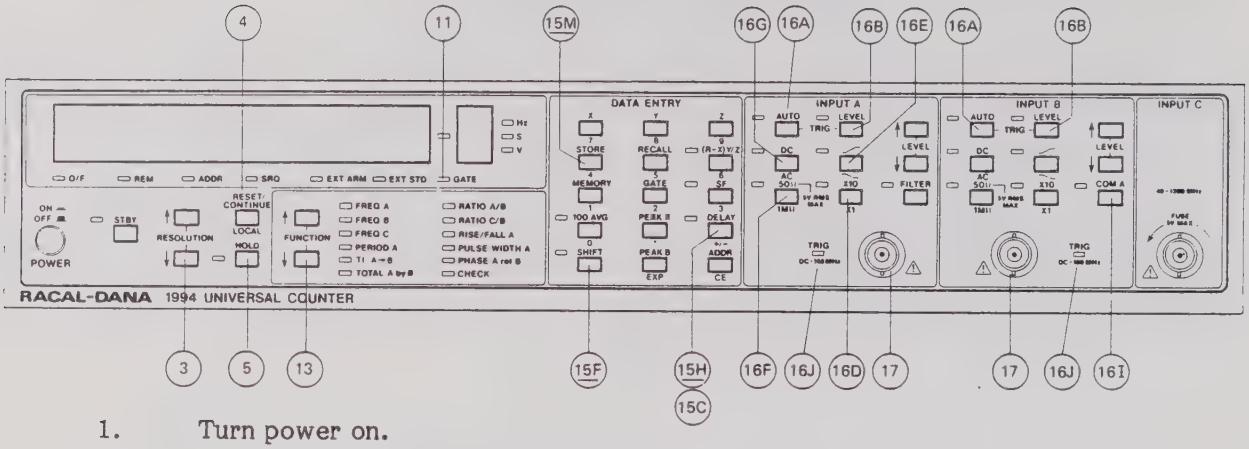
Table 3.4 - Period Measurement (Cont'd)

11. Select the HOLD mode (5) for single-shot measurements. Press the RESET (4) while in Hold to trigger a new measurement.

12. If external arming/gating is in use, trigger a measurement period.

13. Ensure that the GATE LED (11) turns on during the measurement period.

Table 3.5 - Time Interval Measurement



1. Turn power on.

2. Select TI A→B using FUNCTION keys (13).

3. Set the AC/DC coupling (16G) and input impedance (16F) as required.

4. Select the X10 input attenuation (16D) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Select the slope (16E) for Inputs A/B as required. If the start and stop signals are from the same source, select COM A (16I).

6. Connect the start signal to INPUT A (17). If a separate source for the stop signal is used, connect the stop signal to INPUT B (17). TI B→A may be measured using Special Function 21.

7. Select AUTO-TRIG A/B (16A), or set the trigger levels A/B manually using key sequence TRIG-LEVEL (16B) +/- (15C) ⟨value⟩ TRIG-LEVEL (16B). Check that Inputs A and B TRIG-LEDs (16J) flash.

8. Use the RESOLUTION ↑↓ keys (3) when the display resolution will exceed 3 digits (100 ns).

NOTE:

The 1994's resolution is selectable down to 3 digits; however, the counter will display 1 digit when measurements to 0 ns are made.

9. If delayed arming of the stop circuit is required, enter the delay into memory using key sequence ⟨value⟩ SHIFT (15F) STORE (15M) DELAY (15H). Enable the delay using key sequence SHIFT (15F) DELAY (15H). Refer to Subsection 3.4.5 for explanation of delayed stop arming.

Table 3.5 - Time Interval Measurement (Cont'd)

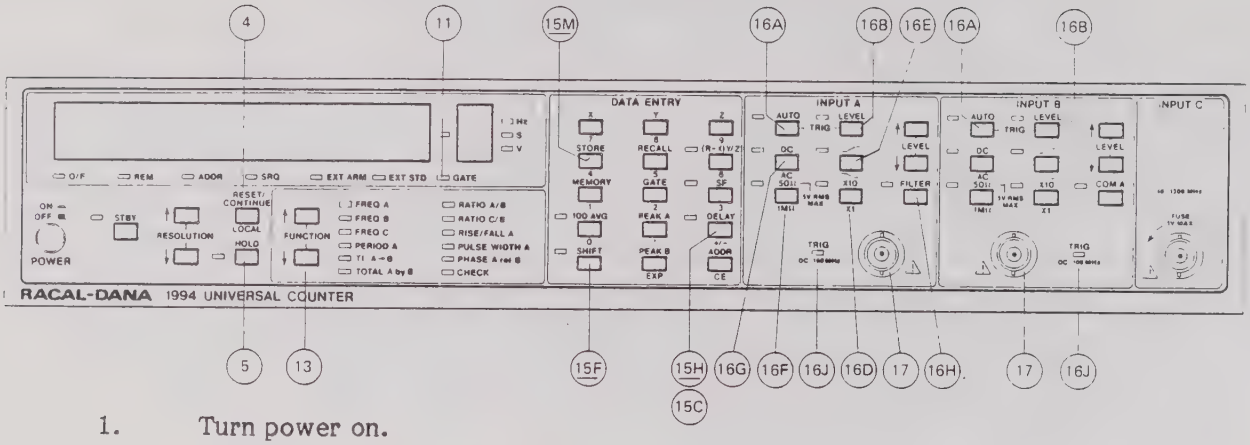
10. If external arming/gating is needed, connect the arming/gating signal and enter the required special function number. Enable special functions. Refer to Subsection 3.4.10 for special function numbers and procedures.

11. Select the HOLD mode (5) for single-shot measurements. Press the RESET (4) while in Hold to trigger a new measurement.

12. If external arming/gating is in use, trigger a new measurement.

13. Ensure that the GATE indicator (11) turns on during the measurement period.

Table 3.6 - Total A by B Measurement



1. Turn power on.

2. Select TOTAL A by B using FUNCTION keys (13).

3. Select the AC/DC coupling (16G) and input impedance (16F) as required.

4. Select the X10 input attenuation (16D) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Select the slopes (16E) as required.

NOTE:

Input A slope selects the slope of the events to be totalized. The measurement period, however, starts on Input B slope and stops on the opposite slope.

6. Connect the signal to be totalized to INPUT A (17) and the control signal to INPUT B (17). TOTAL B by A may be measured using Special Function 21.

7. Select AUTO-TRIG A/B (16A), or set the trigger levels A/B manually using key sequence TRIG-LEVEL (16B) +/- (15C) <value> TRIG-LEVEL (16B). Check that Inputs A and B TRIG LEDs (16J) flash.

8. If a frequency below 50 kHz is to be measured in the presence of high frequency noise, select the FILTER (16H).

9. If delayed arming of the stop circuit is required, enter the delay into memory using key sequence <value> SHIFT (15F) STORE (15M) DELAY (15H). Enable the delay using key sequence SHIFT (15F) DELAY (15H). Refer to Subsection 3.4.5 for explanation of delayed stop arming.

10. If external arming/gating is needed, connect the arming/gating signal and enter the required special function number. Enable special functions. Refer to Subsection 3.4.10 for special function numbers and procedures.

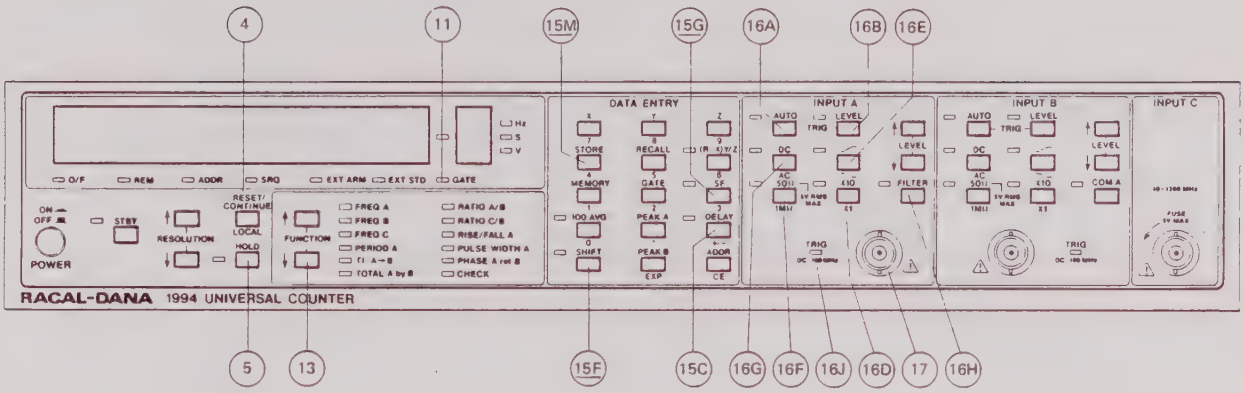
Table 3.6 - Total A by B Measurement (Cont'd)

11. Select the HOLD mode (5) for single-shot measurements. Press the RESET (4) while in Hold to trigger a new measurement.

12. If external arming/gating is in use, trigger a new measurement cycle.

13. Ensure that the GATE indicator (11) turns on during the measurement period.

Table 3.7 - Manual Totalize Measurement



1. Turn power on.

2. Select TOTAL A by B using FUNCTION keys (13).

3. Select the AC/DC coupling (16G) and input impedance (16F) as required.

4. Select the X10 input attenuation (16D) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Select the slope (16E) as required.

6. Enter Special Function 61 using key sequence 61 SHIFT (15F) STORE (15M) and SF (15G). Enable special functions using key sequence SHIFT (15F) SF (15G).

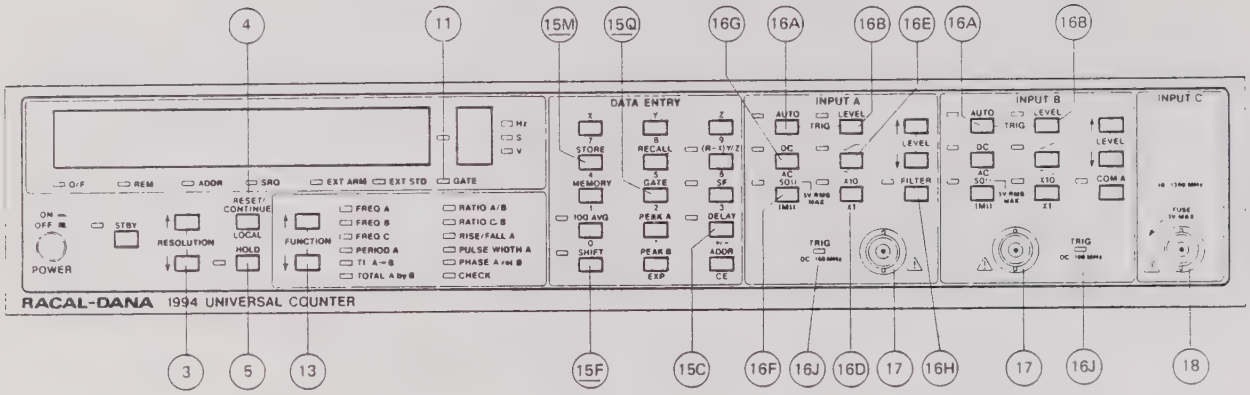
7. Connect the measurement signal to INPUT A (17).

8. Set the AUTO-TRIG A (16A), or select the trigger level A manually using key sequence TRIG-LEVEL (16B) +/- (15C) <value> TRIG-LEVEL (16B). Check that Input A TRIG-LED (16J) flashes.

9. If a frequency below 50 kHz is to be measured in the presence of high frequency noise, select the FILTER (16H).

10. Operate the HOLD key (5). Verify that the count stops and the GATE LED (11) is off. The displayed result is cumulative over successive measurement cycles. Use the RESET key (4) to clear the display. Check that the main display blanks before triggering new measurement cycles.

Table 3.8 - Ratio A/B and C/B Measurements



1. Turn power on.

2. Select RATIO A/B or RATIO C/B using FUNCTION keys (13).

3. Set the AC/DC coupling (16G), input impedance (16F), and slope(s) (16E) as required.

4. Select the X10 input attenuation (16D) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Connect one signal to INPUT B (17) and the other to INPUT A (17) or INPUT C (18). The lower frequency signal should be connected to INPUT B.

6. Select a specific gate time (valid range of 200 µs to 99.9 s) if desired. For small numbers, enter the gate-time using the exponential format. The displayed gate time will be rounded to the nearest 25.6 µs. Use key sequence <value> SHIFT (15F) STORE (15M) GATE (15Q). Programmed gate times are immediately enabled with the resolution set accordingly. Skip step 7 if step 6 is being used to enter the gate time.

7. Use the RESOLUTION ↑↓ keys (3) to select the required display resolution and gate time if step 6 was not used (see Table 3.12).

8. If RATIO A/B is selected, either set trigger levels A and B manually using key sequence TRIG-LEVEL (16B) +/- (15C) <value> TRIG-LEVEL (16B), or select AUTO-TRIG A and B (16A). Check that Inputs A and B TRIG LEDs (16J) flash. For RATIO C/B, a trigger level for only INPUT B may be specified.

9. If a frequency below 50 kHz is to be measured in the presence of high frequency noise, select the FILTER (16H).

Table 3.8 - Ratio A/B and C/B Measurements (Cont'd)

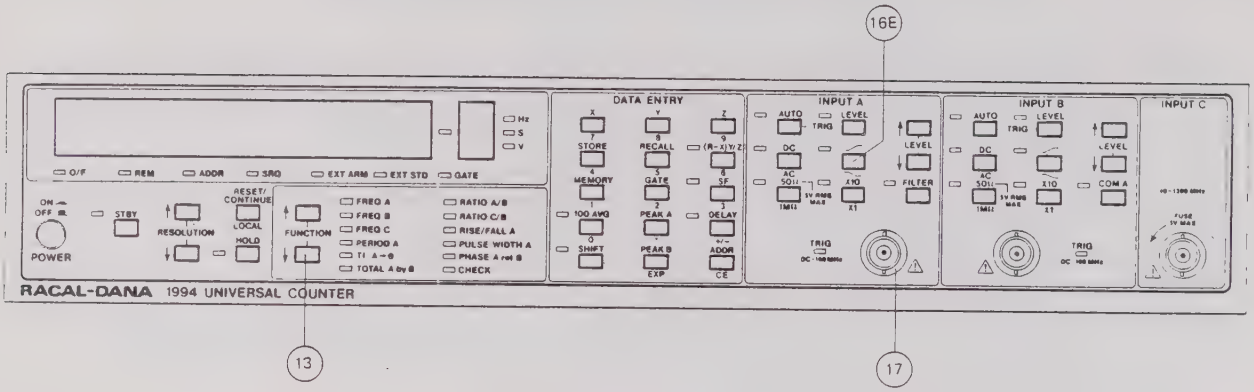
10. If external arming/gating is needed, connect the arming/gating signal and enter the required special function number. Enable special functions. Refer to Subsection 3.4.8 for function numbers and procedures.

11. Select the HOLD mode (5) for single-shot measurements. Press the RESET (4) while in HOLD to trigger a new measurement.

12. If external arming/gating is in use, trigger a new measurement cycle.

13. Ensure that the GATE indicator (11) turns on during the measurement period.

Table 3.9 - Rise/Fall A Measurements



1. Turn power on.

2. Select RISE A (default state) using the FUNCTION keys (13). Input A trigger slope is positive (⎍).

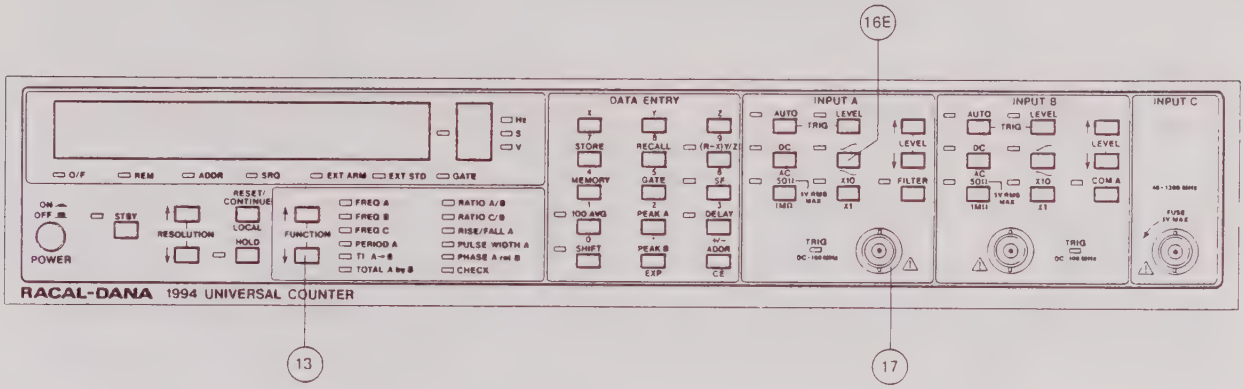
3. Use the slope key for Input A (16E) to change RISE A to FALL A by toggling Input A slope to negative (⎏).

4. Connect measurement signal to INPUT A (17).

NOTE:

All other controls are set automatically.

Table 3.10 - Pulse Width A Measurement



1. Turn power on.

2. Select PULSE WIDTH A using FUNCTION keys (13). Default state is positive pulse width with start-positive and stop-negative 50% trigger points.

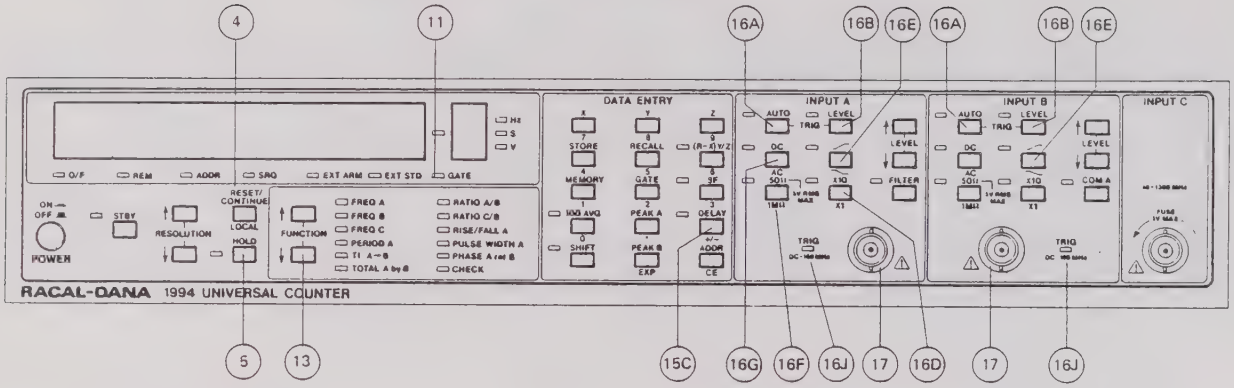
3. Use the slope key for Input A (16E) to change to negative pulse width by toggling Input A slope to negative (⌞). Negative pulse width has start-negative and stop-positive 50% trigger points.

4. Connect measurement signal to INPUT A (17).

NOTE:

All other controls are set automatically.

Table 3.11 - Phase A rel B Measurement



1. Turn power on.

2. Select PHASE A rel B using FUNCTION keys (13).

3. Set the AC/DC coupling (16G), input impedance (16F), and slopes (16E) as required. Selected slopes for signals A and B should be the same.

4. Select the X10 input attenuation (16D) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Connect the signals to be compared to INPUT A (17) and INPUT B (17).

6. Select AUTO-TRIG A and B (16A), or set the trigger levels A and B manually using key sequence TRIG-LEVEL (16B) +/- (15C) <value> TRIG-LEVEL (16B). Check that Inputs A and B TRIG LEDs (16J) flash.

7. Ensure that the GATE indicator (11) turns on during the measurement period.

NOTE:

A phase measurement is always positive, representing the angle by which Input A's signal leads that of Input B. The signals for phase measurement must be continuous and have the same frequency.

3.4.2 Trigger Level Setting

3.4.2.1 Introduction

3.4.2.1.1 Refer to Figure 3.1 for this subsection. The 1994 provides both manual and automatic (including single-shot) trigger setting for Inputs A and B. Trigger level readout is available on the main display.

3.4.2.1.2 Manual trigger selection involves setting the levels in either the ±5.1V or ±51V ranges, with corresponding resolutions of 20 mV and 200 mV. These ranges correspond to attenuation settings of X1 and X10. Any valid trigger entry, having more than 3 digits will be entered but truncated to just 3 digits when stored as a trigger level. For example, 4.6432V becomes 4.64V (X1), or 4.6V (X10). Also, the trigger level operates in 20 mV (X1) and 200 mV (X10) steps with all entries being rounded up. For example, 1.3754V becomes 1.38 (X1) and 1.4 (X10).

3.4.2.1.3 Auto-trigger level is the mean of the positive and negative-peak values of the input signal as automatically determined by the counter.

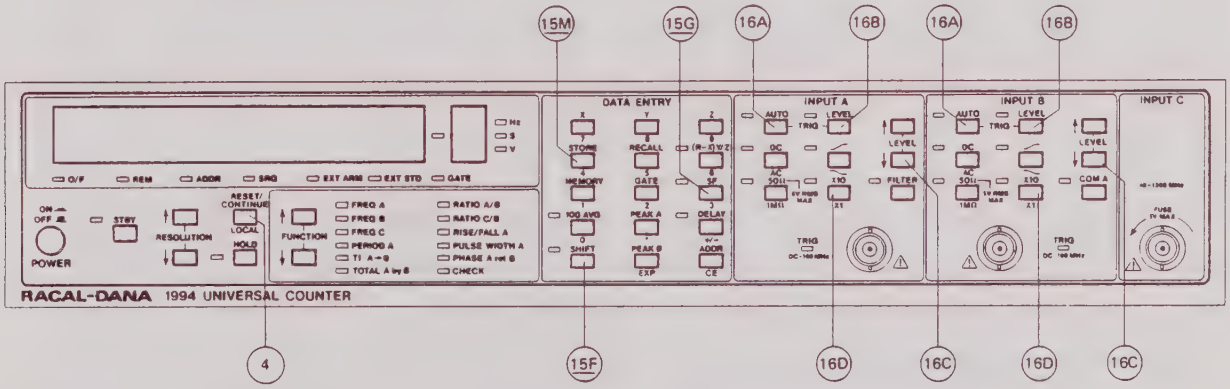


Figure 3.1 - Trigger Level Setting

3.4.2.2 Manual Trigger Setting

NOTE:

An attenuation setting of X1 and a trigger level of 1.24 volts are used in the following description.

3.4.2.2.1 Set the trigger level manually using one of the following key sequences:

a. To set a trigger level of +1.24, use TRIG-LEVEL (16B) <1.24>
TRIG-LEVEL (16B)

b. To set a trigger level of -1.24, use TRIG-LEVEL (16B) +/- (15C) <1.24>
TRIG-LEVEL (16B)

3.4.2.2.2 Pressing the TRIG-LEVEL key (16B) displays Input A or B's current trigger level and causes the TRIG-LEVEL LED to flash.

3.4.2.2.3 This displayed trigger level can now be changed up (↑) or down (↓) in 20 mV steps (X1) or 200 mV steps (X10) using either the LEVEL ↑↓ keys (16C), or a new trigger level entered from the keyboard.

3.4.2.2.4 Press the TRIG-LEVEL key (16B) again to return the counter to its main function and store the displayed trigger level. The TRIG-LEVEL LED should stop flashing. The key sequence for manual trigger level step-up/down and store is TRIG-LEVEL (16B) LEVEL ↑↓ (16C) TRIG-LEVEL (16B).

3.4.2.2.5 Any manual trigger level that is out-of-range will produce an "Op Er" display message. For example, entering 47.2V as a trigger level in X1 attenuation will generate an "Op Er" display message. The operator should press the CONTINUE key (4) to return to the previous trigger setting in the measurement mode; select X10 attenuation (16D); press the TRIG-LEVEL key (16B) to display the trigger level; reenter 47.2V. This new trigger level may be stored or changed.

NOTE:

INPUT A and B each have a single trigger-level store. Using the Auto-Trigger mode overwrites a manually stored trigger setting. Also, pressing the AUTO-TRIG key (16A) while manually setting the trigger level enables the Auto-Trigger mode. Toggle the AUTO-TRIG key (16A) off, then enter a manual trigger level.

3.4.2.3 Automatic Trigger Setting

3.4.2.3.1 Press the required AUTO-TRIG key (16A) to calculate and set the auto-trigger level. Automatic attenuation occurs in the Auto-Trigger mode.

3.4.2.3.2 Press the corresponding TRIG-LEVEL key (16B) to display the auto-trigger level. The TRIG-LEVEL LED will flash when the trigger level is being displayed.

3.4.2.4 Single-Shot Automatic Trigger

3.4.2.4.1 Automatic trigger settings vary as peak input levels change. To execute and store a single-shot auto-trigger level:

a. Enter Special Function 31 using key sequence 31 SHIFT (15F) STORE (15M) and SF (15G)

b. Enable special functions using key sequence SHIFT (15F) SF (15G)

c. Press the AUTO-TRIG key (16A). The LED lights as the level is calculated and set, then turns off

3.4.2.4.2 The stored level is retained as a manually set value until either (1) another single-shot measurement is made, or (2) a new manual trigger level is entered.

3.4.2.4.3 To execute additional single-shot trigger settings, press the AUTO-TRIG key (16A) again with Special Function 31 enabled.

3.4.2.5 Automatic Attenuation Setting

3.4.2.5.1 When operating in the Auto-Trigger mode, automatic switching of the X10 attenuator occurs as follows:

a. The attenuator is selected if the peak-to-peak value of the input signal exceeds 5.1V or if either peak is outside the range ±5.1V

b. The attenuator is deselected if the peak-to-peak value of the input signal is less than 4.6V and both peaks are within the range ±4.6V

3.4.3 Display Resolution

3.4.3.1 In the 1994, except for totalize and phase, resolution for all functions refers to the number of displayed zeros when no input signal is being applied. Resolution of totalize and phase measurements is determined by the input signal. (Resolution of time interval, rise/fall, and pulse width is determined by both the resolution set and input signal.)

3.4.3.2 The 1994's resolution can be set to any value from 3 to 10 digits. For a resolution of 10, the most significant digit will overflow the display. A 10% overrange of the counter's display occurs without a change of range.

3.4.3.3 Results are rounded to meaningful values in all measurement functions. Therefore, the number of displayed digits may be less than the selected resolution. For example, in the time-interval function, the resolution may be selected down to 3 digits (100 ns); however, the 1994 will display only 1 digit when measuring down to 0 ns.

3.4.3.3.1 In frequency ratio, a maximum of 7 digits are displayed regardless of the selected resolution.

3.4.3.3.2 In totalize, the display shows the true total of events counted from 1 to 999999999. For higher totals (ranges of 1 to 10E18), an exponential display is used.

3.4.3.3.3 In phase, a maximum of 4 digits are displayed for frequencies to 1 MHz; 3 digits for higher frequencies. Any leading zeros are blanked. For frequencies above 10 MHz, the display resolution is 10^{0} with a place-holding zero displayed as the least-significant digit.

3.4.3.4 Display Resolution Setting

3.4.3.4.1 Display resolution for the 1994 is function-dependent and is set using the RESOLUTION ↑↓ keys to select the number of display digits from 3 to 10 (9 plus overflow). To step up from 9 to 10 digits, the RESOLUTION ↑ key must be held down for about two seconds. The exponent digit will be set to zero when a 10-digit resolution is selected.

3.4.4 Gate Time

3.4.4.1 Refer to Table 3.12. In frequency, period, ratio, and check functions, the gate time is set by the selected resolution.

Table 3.12 - Resolution and Gate Time

Resolution (no. of selected digits) in Frequency, Period, Ratio, and Check-See Note 1	Gate Time	Display	GPIB Code
9 + Overflow	10 s	Up Stop	SRS* 10
9	1 s		9
8	100 ms	Default	8
7	10 ms		7
6	1 ms		6
5 ⎫ See	1 ms		5
4 ⎬ Note	1 ms		4
3 ⎭ 2	1 ms	Down Stop	3

NOTE 1:

The most significant digit is permitted to exceed the resolution by 1 digit providing a 10% overrange. This precludes unnecessary shifting of digits.

*SRS=Store Display Resolution Command

NOTE 2:

Measurements of frequency, period, ratio, and check are averaged when these gate times are set.

3.4.4.2 Gate Time Storage/Recall

3.4.4.2.1 Use key sequences ⟨value⟩ SHIFT STORE GATE and SHIFT RECALL GATE to store and recall gate times, respectively.

3.4.4.3 The default state is determined by the resolution selected (see table above); the home state resolution is 8 digits or a 100-ms gate time.

3.4.4.4 Also, gate times may be programmed in increments rounded to the nearest 25.6 µs using the range of 200 µs to 99.9 s. Whenever the counter is not in the resolution mode and gate times are being set directly, the display resolution is dependent on the input signal's frequency/time and gate time.

3.4.4.5 Gate time may be extended over the programmed value as follows:

a One period of the input signal on FREQ B, RATIO A/B

b. Two periods of the input signal on FREQ A, PERIOD A

3.4.4.6 When the counter's gate time is programmed, it is immediately enabled. Pressing the RESOLUTION ↑↓ keys will disable the gate time which reverts to the nearest decade.

3.4.5 Stop Arm Delay (Hold Off)

3.4.5.1 The arming of the stop input circuit may be delayed or held off when either the TI A→B or TOTAL A by B function is selected. The programmable delay range is 200 μs to 800 ms, with the display rounded to the nearest 25.6 μs. In the home state, the delay function is set at its minimum value of 200 μs.

3.4.5.2 The stop arm delay can be useful in preventing premature triggering of the stop circuit by spurious signals (e.g., those resulting from relay contact bounce). Figure 3.2 below shows the principle of the stop arm delay.

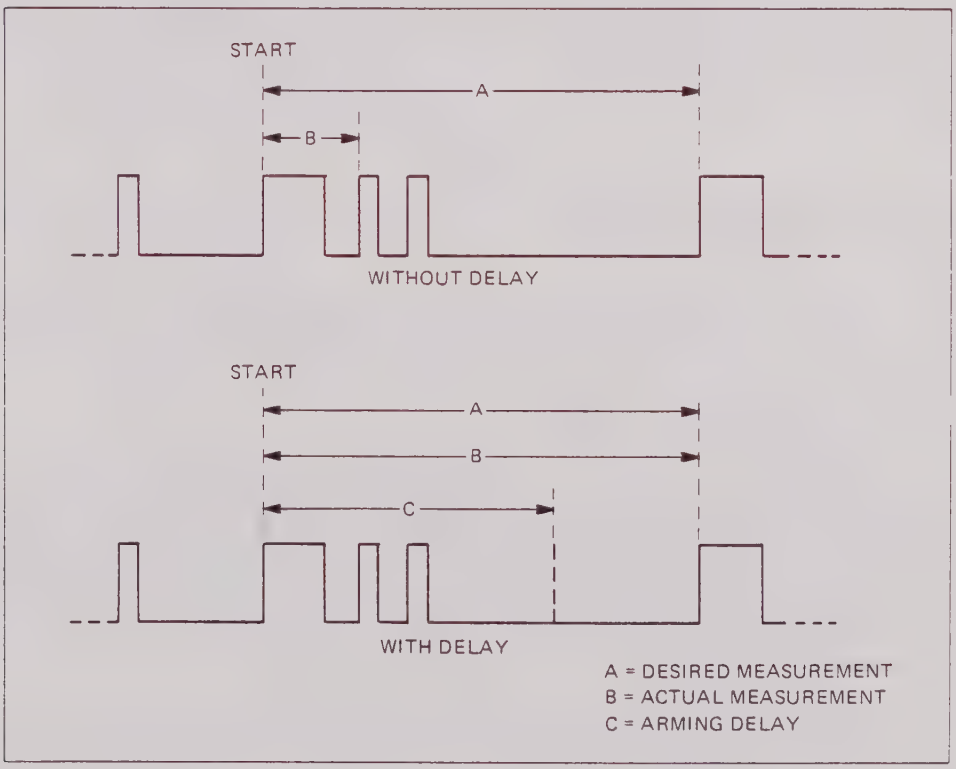


Figure 3.2 - Use of Stop Arm Delay

3.4.5.3 Stop Arm Delay Storage

3.4.5.3.1 A stop arm delay is stored using key sequence ⟨value⟩ SHIFT STORE DELAY, where ⟨value⟩ is in decimal or exponential form.

3.4.5.3.2 The value of the displayed delay entered is rounded to the nearest 25.6 μs before it is stored. Attempted entry of an out-of-range value will result in an "Op Er" being displayed. The stored delay is retained when the counter is placed in the Standby mode. The counter returns to the measurement mode automatically once the delay value is entered.

3.4.5.4 Stop Arm Delay Recall

3.4.5.4.1 Recall stored delay values to the display using key sequence SHIFT RECALL DELAY.

3.4.5.5 Stop Arm Delay Enabling/Disabling

3.4.5.5.1 Enable and disable the stop arm delay by successively using key sequence SHIFT DELAY. The LED lights when the delay function is enabled.

3.4.6 Math Function (R-X) Y/Z

3.4.6.1 The math function applies to all counting and timing functions of the 1994 except phase measurement and check. This function permits measurement value R to be offset, normalized, or scaled before display, using stored constants X, Y, and/or Z, respectively. The display indicates (R-X) Y/Z after enabling the math function. Home state values for X, Y, and Z are 0, 1, and 1, respectively ($Z \neq 0$ at any time).

NOTE:

It is possible to store a 0 for constant Z. However, Error 20 will result if the math function is enabled with this value set.

3.4.6.2 Because the 1994 attempts to retain engineering format in its display, one or two small place-holding zeros will be shown when a computation causes the display to exceed counter resolution.

3.4.6.3 Math Constant Storage/Recall

3.4.6.3.1 Constants X, Y, and/or Z must be stored before enabling the math function. Use key sequence ⟨value⟩ SHIFT STORE X/Y/Z, where ⟨value⟩ is in decimal or exponential form, to enter any of the constants. The permissible range of values for the math constants is ±0.000000001 E-9 to ±10000000000 E9 to nine significant digits. Any number exceeding this range will result in an "Op Er" being displayed. The actual display range for the 1994 is ±999.999999 E±9. Use key sequence SHIFT RECALL X/Y/Z to recall math constants.

3.4.6.3.2 The counter returns to the measurement mode automatically once the value for the constant is entered.

3.4.6.4 Displayed Reading Storage

3.4.6.4.1 Use key sequence <R> SHIFT STORE X/Y/Z, to store displayed reading <R> into either the X/Y/Z register.

3.4.6.5 Math Function Enabling/Disabling

3.4.6.5.1 Enable and disable the math function by successively using key sequence SHIFT (R-X)Y/Z. The LED lights when the math function is enabled.

3.4.7 Memory Function

3.4.7.1 Refer to Table 3.1, Ref. 15P for details.

3.4.8 Peak Level Recall

3.4.8.1 Press key sequence SHIFT RECALL PEAK A/PEAK B. The display shows the positive and negative peaks of A or B. Using this feature requires Auto-Trigger selected.

3.4.9 100 AVG Function

3.4.9.1 This function permits the counter to accumulate 100 measurements and display the averaged result. The function may be applied to all counting and timing functions of the 1994 except totalize. Resolution is improved by one display digit (one decade). Any number exceeding the display range will produce an "Er 02" error message.

3.4.9.2 100 AVG Function Enabling/Disabling

3.4.9.2.1 Enable and disable the 100 AVG function by successively using key sequence SHIFT 100 AVG. The LED lights when the 100 AVG function is enabled.

3.4.10 Special Functions

3.4.10.1 Table 3.13 lists the special functions available on the 1994. All special functions are designated by a two-digit special function number (NN).

3.4.10.2 Special functions are organized by decades, one for each of the nine mantissa display digits. One special function from each decade is entered into a special function register. Only the second digit is stored; the decade is indicated by the position of the digit in the register. Default state has a 0 entered in each position. To recall the special functions setup, use key sequence SHIFT RECALL SF. Refer to Figure 3.3 for a typical special functions display.

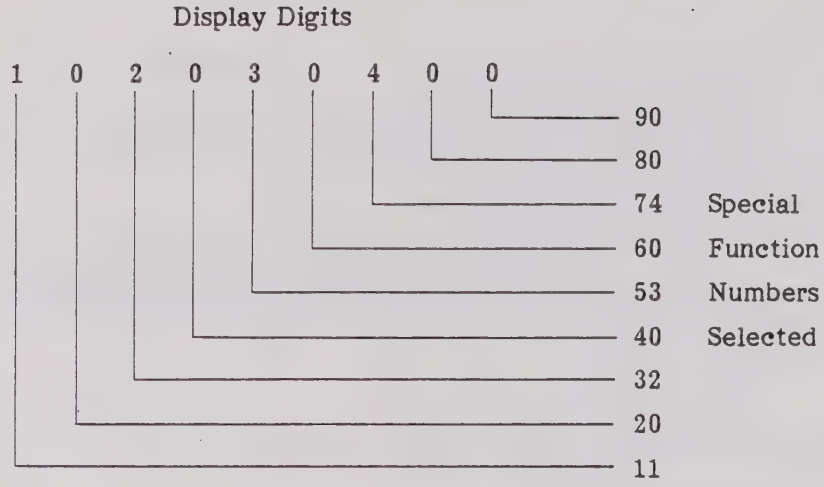


Figure 3.3 - Special Function Register Display

3.4.10.3 Special Function Storage

3.4.10.3.1 Special function numbers must be entered into memory before special functions can be enabled. Use the following key sequence to store, for example, special function 21: 21 SHIFT STORE SF.

3.4.10.3.2 The digits for a special function number are shown on the display as the numeric keys are pressed. Once the number is stored, the counter automatically returns to the measurement mode.

3.4.10.3.3 When a number is stored, it overwrites the number stored in the same decade. Therefore, to remove a number from its register, another number from the same decade must be stored.

3.4.10.3.4 Numbers stored in the special function register are retained when the counter is switched to Standby mode and as a front-panel setting in Recall Memory mode.

3.4.10.4 Special Function Recall

3.4.10.4.1 Stored special functions are recalled for display using key sequence SHIFT RECALL SF.

3.4.10.5 Special Function Enabling/Disabling

3.4.10.5.1 The power-on home state for special functions is that none are stored. Default state then corresponds to the special function register, with all digits displaying zero. Successively use key sequence SHIFT SF to enable and disable stored special functions. The LED lights when special functions are enabled.

NOTE:

Storing a special function when special functions are enabled immediately enables that special function.

Table 3.13 - Special Functions (SFs)

SF Number		Function		
			Start	Stop
10	Arming	Default:	Internal	Internal
11			External+ve	Internal
12			External-ve	Internal
15			External+ve	External+ve
16			External+ve	External-ve
17			External-ve	External+ve
18			External-ve	External-ve
20		Default:	Normal Operation	
21			Inputs A and B interchanged. Permits PERIOD B and TI B→A measurements, for example.	
			See Note 1 below:	
30		Default:	Continuous auto-trigger measurement	
31			Single-shot auto-trigger measurement	
40	Display Time between measurement cycles	Default:	Rdg. update rate x 150 ms	
41			Rdg. update rate maximum	
42			1s read rate	
43			10s read rate	
44			300s read rate	
			See Note 2 below:	
60		Default:	Totalize A by B	
61			Manual Totalize	
70		Default:	Basic 10 MHz Check/Press CHECK key	
71			LED Check/Press CHECK key	
72		Diagnostic Testing	Start TEC short continuous calibration (100 ns pulse applied); display shows TEC count	
73			Start TEC long continuous calibration (200 ns pulse applied); display shows TEC count	
74			Stop TEC short calibration	
75			Stop TEC long calibration	
76			Input A and B DAC Check-continuously ramps through DACs	
77			Input A relay check/Press CHECK key	
78			Input B relay check/Press CHECK key	
			See Note 3 below:	

Table 3.13 - Special Functions (SFs) (Cont'd)

SF Number	Function
	NOTE 1: In Special Function 21, Frequency B is specified to 100 MHz only; Period B is specified to 10 ns only; Totalize B by A operates for one complete cycle of Input A.
	NOTE 2: Special Functions 40, 42, 43, and 44 are available only in local operation. Special Function 41 is selected automatically when in remote operation.
	NOTE 3: Special Functions 77 and 78 require connection of a 10 MHz internal standard to Input A or B.

3.4.11 Error Codes

3.4.11.1 Table 3.14 lists the error codes that may be displayed by the counter during local operation. All errors will be displayed either as "Er NN" where NN is a 2-digit code number, or simply as "Op Er". Error codes will clear from the display as described in par. 3.4.11.2.

Table 3.14 - Error Codes

Displayed Codes	Error
Er 01	Signals of different frequencies used in phase measurement
Er 02	Measurement result too large or too small to display
Er 03	Overflow of internal counters
Op Er	Numerical entry error (e.g., number out-of-range or attempt to store trigger level in an auto-triggered channel)
—	Programming error
Er 50	Basic Check mode error
Er 51	Relay Check Failure — Input A: X1/X10; 50Ω/1 MΩ; AC/DC; FILTER in/out; COM A
Er 52	
Er 53	
Er 54	
Er 55	
Er 56	Relay Check Failure — Input B: X1/X10; 50Ω/1 MΩ; AC/DC
Er 57	
Er 58	
	NOTE: Er 51-58 only occur in the Check and Special Function 71-78 modes.

3.4.11.2 Error Code Clearance

3.4.11.2.1 Error code "Er 01" is cleared by:

a. Performing a phase measurement on signals of equal frequency

b. Choosing another measurement function

3.4.11.2.2 Error codes "Er 02" and "Er 03" are cleared by:

a. Obtaining a measurement result that is within range

b. Choosing another measurement function

3.4.11.2.3 "Op Er" is cleared by pressing the RESET key.

SECTION 4 SYSTEM OPERATION

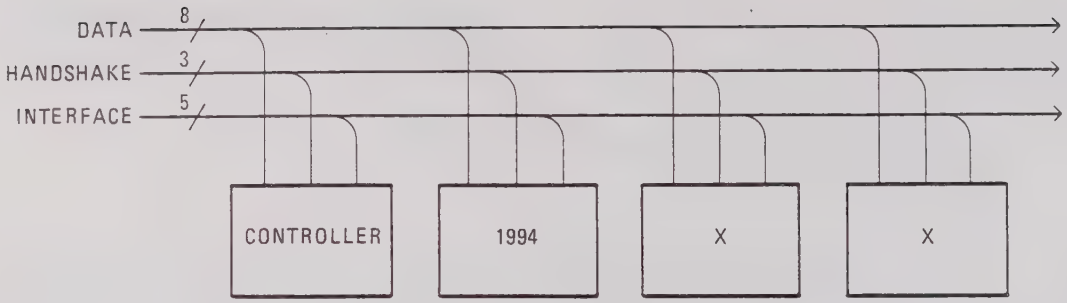
4.1 GENERAL PURPOSE INTERFACE BUS (GPIB)

4.1.1 Introduction

4.1.1.1 This subsection provides operating information for the 1994 using the GPIB interface. The IEEE-488-1978 interface permits remote control of all the counter's functions except POWER ON/OFF and STBY. Inputs and outputs are made via a standard 24-pin connector (see Figure 4.1) on the rear panel. Pin location, signal line identification, and GPIB operation comply with IEEE-STD-488-1978. The GPIB provides interface capability with other instruments and a controller also using the interface-bus structure (see Figure 4.2). This figure also shows signal line designations and pin assignments. IEEE-STD-488-1978 subsets available are listed in Table 4.1.

Pin No.	Assignment	Pin No.	Assignment
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	GND, (6)
7	NRFD	19	GND, (7)
8	NDAC	20	GND, (8)
9	IFC	21	GND, (9)
10	SRQ	22	GND, (10)
11	ATN	23	GND, (11)
12	SHIELD	24	GND, (5 AND 17)

Figure 4.1 - GPIB Connector (Rear Panel)



Pin	Nomenclature	Description
1	DIO-1 Data In/Out Bit 1 (LSB)	Data lines are used to transfer data from one instrument to another
2	DIO-2 Data In/Out Bit 2	
3	DIO-3 Data In/Out Bit 3	
4	DIO-4 Data In/Out Bit 4	
13	DIO-5 Data In/Out Bit 5	
14	DIO-6 Data In/Out Bit 6	
15	DIO-7 Data In/Out Bit 7	
16	DIO-8 Data In/Out Bit 8	
6	DAV (Data Valid)	Handshake lines operate in a proper time sequence for complete communication between instruments
7	NRFD (Not Ready for Data)	
8	NDAC (Not Data Accepted)	
5	EOI (End or Identify)	Interface lines are used to provide an orderly flow of information between units
9	IFC (Interface Clear)	
10	SRQ (Service Request)	
11	ATN (Attention)	
17	REN (Remote Enable)	
12	SHIELD	
18	GND (6)	
19	GND (7)	
20	GND (8)	
21	GND (9)	
22	GND (10)	
23	GND (11)	
24	GND (5 and 17)	

Figure 4.2 - Interface Signal Pin Assignments

4.2 GPIB DESCRIPTION

4.2.1 Refer to Figure 4.2. There are 24 lines available at the GPIB connector, including 16 signal and 7 ground return lines, and one shield. All of the data bus lines are either input or output lines, having the following characteristics:

Logic Levels:	1 = Low = $\leq$.8V
	0 = High = $\geq$2.0V
Input Loading:	Each input = one TTL load
Output:	The output is capable of driving 15 interface bus loads. It consists of an open-collector driver and is capable of sinking 48 mA with a maximum voltage drop of 0.4 volts. See the IEEE-488 Electrical Specifications.

Table 4.1 - IEEE-488-1978 Standard Interface Subset Capability

GPIB Subset	Description	Applicable Capability
SH1	Source Handshake	Complete Capability
AH1	Acceptor Handshake	Complete Capability
T5	Talker (1) (2) (3) (4)	Complete Capability Basic Talker Serial Poll Talk Only Mode Unaddress if MLA
TE0	Extended Talker	None
L4	Listener (1) (2)	Complete except Listen Only Basic Listener Unaddress if MTA
LE0	Extended Listener	None
SR1	Service Request	Complete Capability
RL1	Remote/Local (1) (2) (3)	Complete Capability REN - Remote Enable LL0 - Local Lockout GTL - Go to Local
PP0	Parallel Poll	No Capability
DC1	Device Clear (1) (2)	Complete Capability DCL - Device Clear SDC - Selected Device Clear
DT1	Device Trigger	Complete Capability GET - Group Execute Trigger
C0	Controller	No Capability
E1	Open Collector Bus Drivers	

4.2.2 The signal lines shown in Figure 4.2 consist of three functionally separate sets: Data, Handshake, and Interface.

4.2.2.1 **Data** - the data lines consist of DIO-1 to DIO-8. These lines are the signal channels over which data flows between all instruments on the bus in bit-parallel, byte-serial form.

4.2.2.2 **Handshake** - these three transfer lines consist of: DAV (Data Valid), NDAC (Not Data Accepted), and NRFD (Not Ready for Data). These lines provide communication between GPIB bus members (i.e., between the instrument that is talking and the instrument(s) that are listening) to synchronize the information flow across the eight data lines. These lines derive their nomenclature from their meaning in the low or 1 state (e.g., when NRFD is low, the device is Not Ready for Data).

a. **DAV** - when low, it signifies that valid information is available on the data lines

b. **NRFD** - when low, it signifies that the instrument is not ready to accept information

c. **NDAC** - when low, it signifies that information is not accepted by the acceptor bus device

4.2.2.3 **Interface** - these five interface lines coordinate the information flow on the bus.

a. **IFC (Interface Clear)** - places the instrument in the Idle state (i.e., Untalk, Unlisten)

b. **ATN (Attention)** - indicates the kind of information on the data lines during a handshake transfer sequence. Low indicates data lines carry interface commands; high indicates that the data lines carry data

c. **REN (Remote Enable)** - arms the instrument to select Remote operation when it's addressed as a listener

d. **SRQ (Service Request)** - signals the system controller that a peripheral device or bus member wants attention for purposes such as transmitting measurement, status, or condition information to the system controller

e. **EOI (End or Identify)** - used for (1) signifying the end of a message and (2) together with ATN, signalling bus peripherals to set the I/O bit assigned for parallel poll identification

4.2.3 GPIB Handshake

4.2.3.1 The handshake sequence is the process by which each data byte is transferred from the source to the acceptor.

4.2.3.2 Refer to Figure 4.3. It shows the sequential relationship between the DAV, NRFD, and NDAC lines used to transfer data bytes. Figure 4.4 shows the handshake flow chart.

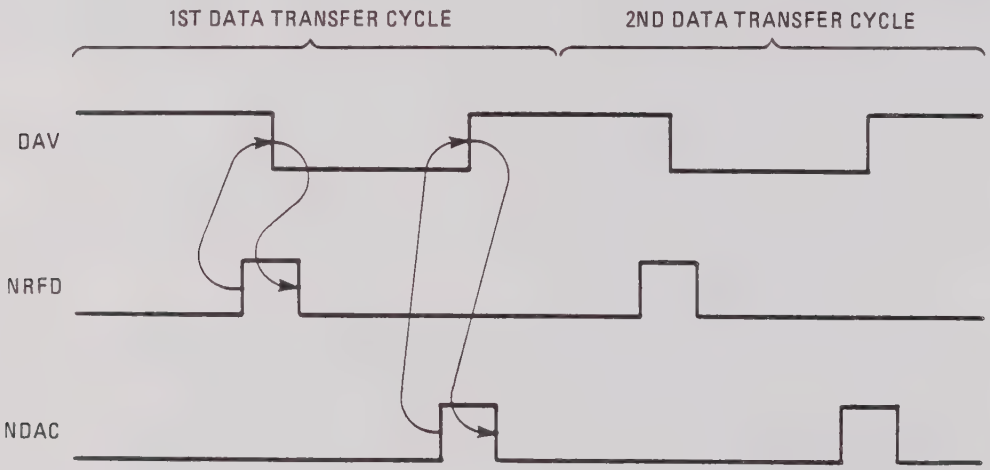


Figure 4.3 - Handshake Sequence

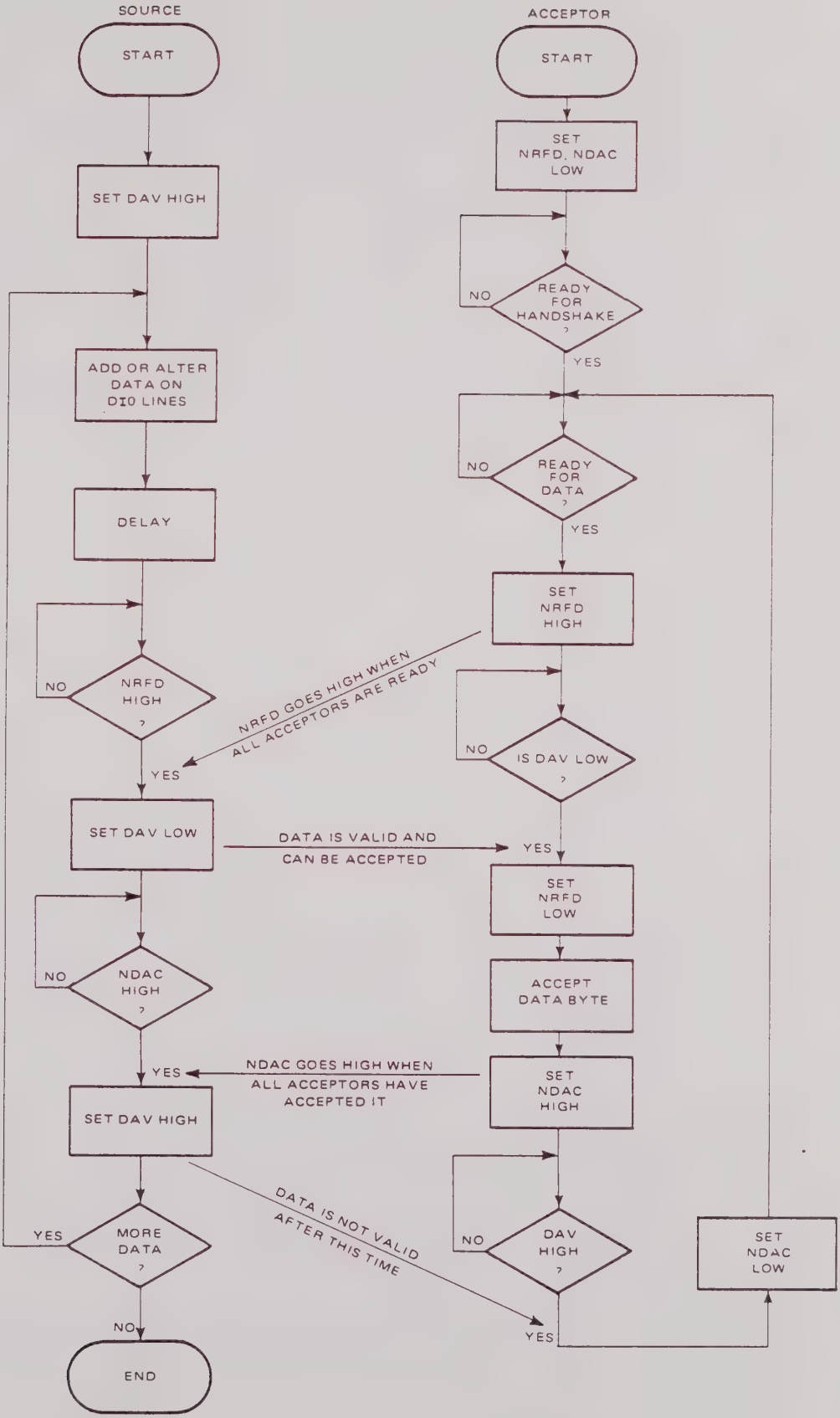


Figure 4.4 – Handshake Flow Chart

4.3 GPIB ADDRESS ASSIGNMENT

4.3.1 The 1994 must be assigned an address as a bus member when operating in a GPIB system. Assigning an address to the counter permits it to be "called up" by the system controller or other resident bus device without interfering with them.

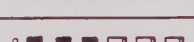
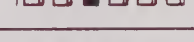
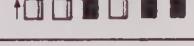
NOTE:

Only a total of 15 devices, including the 1994, can reside on any single 488-bus.

4.3.2 The counter is equipped with a rear-panel switch bank, enabling the user to assign one of 31 addresses (numbers 00 to 30).

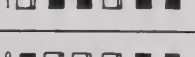
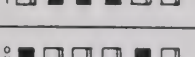
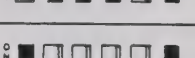
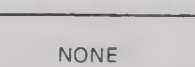
4.3.3 Table 4.2 contains all the information required for setting the counter's address and determining the talk and listen address codes used in programming the controller.

Table 4.2 - 1994 GPIB Address Assignment

ASCII CHARACTERS		DATA LINES							ADDRESS SWITCH SETTING **	DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	TALK ONLY 1 / 0; A5 A4 A3 A2 A1; switches 1 2 3 4 5 6	
TALK	LISTEN	TALK	LISTEN	ADDRESS						
				16	8	4	2	1		
	SP	0	1	0	0	0	0	0		00
@		1	0	0	0	0	0	0		
	!	0	1	0	0	0	0	1		01
A		1	0	0	0	0	0	1		
	"	0	1	0	0	0	1	0		02
B		1	0	0	0	0	1	0		
	#	0	1	0	0	0	1	1		03
C		1	0	0	0	0	1	1		
	$	0	1	0	0	1	0	0		04
D		1	0	0	0	1	0	0		
	%	0	1	0	0	1	0	1		05
E		1	0	0	0	1	0	1		
	&	0	1	0	0	1	1	0		06
F		1	0	0	0	1	1	0		
	' (APOSTROPHE)	0	1	0	0	1	1	1		07
G		1	0	0	0	1	1	1		
	(	0	1	0	1	0	0	0		08
H		1	0	0	1	0	0	0		
	)	0	1	0	1	0	0	1		09
I		1	0	0	1	0	0	1		
	*	0	1	0	1	0	1	0		10
J		1	0	0	1	0	1	0		
	+	0	1	0	1	0	1	1		11
K		1	0	0	1	0	1	1		
	,	0	1	0	1	1	0	0		12
L		1	0	0	1	1	0	0		
	-	0	1	0	1	1	0	1		13
M		1	0	0	1	1	0	1		
	.	0	1	0	1	1	1	0		14
N		1	0	0	1	1	1	0		
	/	0	1	0	1	1	1	1		15
O		1	0	0	1	1	1	1		

**The "Talk Only" switch is set to "ON" when used with a printer or other "listen only" device.

Table 4.2 – 1994 GPIB Address Assignment (Cont'd)

ASCII CHARACTERS		DATA LINES							ADDRESS SWITCH SETTING **	DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	TALK ONLY 1 / 0 — A5 A4 A3 A2 A1	
TALK	LISTEN	TALK	LISTEN	ADDRESS						
				16	8	4	2	1		
	Ø	0	1	1	0	0	0	0		16
P		1	0	1	0	0	0	0		
	1	0	1	1	0	0	0	1		17
Q		1	0	1	0	0	0	1		
	2	0	1	1	0	0	1	0		18
R		1	0	1	0	0	1	0		
	3	0	1	1	0	0	1	1		19
S		1	0	1	0	0	1	1		
	4	0	1	1	0	1	0	0		20
T		1	0	1	0	1	0	0		
	5	0	1	1	0	1	0	1		21
U		1	0	1	0	1	0	1		
	6	0	1	1	0	1	1	0		22
V		1	0	1	0	1	1	0		
	7	0	1	1	0	1	1	1		23
W		1	0	1	0	1	1	1		
	8	0	1	1	1	0	0	0		24
X		1	0	1	1	0	0	0		
	9	0	1	1	1	0	0	1		25
Y		1	0	1	1	0	0	1		
	:	0	1	1	1	0	1	0		26
Z		1	0	1	1	0	1	0		
	;	0	1	1	1	0	1	1		27
[		1	0	1	1	0	1	1		
	<	0	1	1	1	1	0	0		28
\		1	0	1	1	1	0	0		
	=	0	1	1	1	1	0	1		29
]		1	0	1	1	1	0	1		
	>	0	1	1	1	1	1	0		30
^		1	0	1	1	1	1	0		
NONE		ILLEGAL							NONE	31

**The "Talk Only" switch is set to "ON" when used with a printer or other "listen only" device.

4.3.4 Note in the table the column headed "ADDRESS SWITCH SETTING". It illustrates the positions of switches A1 to A5 for each number address listed in the far right column. To set the GPIB address, simply select the desired decimal address for the counter, refer to the table, and set the switches on the address selector to the corresponding pattern shown in the column.

4.3.5 Once an address has been assigned and stored, the controller may then address the 1994 as a talker/listener by transmitting the appropriate ASCII character on the data lines. The "DATA LINES" column of the table shows the 7-bit binary codes for every talk/listen address assigned to the counter. The controller transmits these codes to the counter to establish its talker/listener status.

4.3.6 Note also in the table that there are two address codes for each GPIB address number. Each code represents a different ASCII character. For example, if an address of 02 is assigned to the counter, the talk address is the ASCII character B and the listen address is the ASCII character ". The only difference in the binary code in each case is the state of data lines D6 and D7.

4.3.7 The counter's GPIB address can be displayed in decimal form using key sequence SHIFT RECALL ADDR. If the 1994's bus address is changed, the previous key sequence must be repeated to display the new address. Press the CONTINUE key to return the 1994 to the measurement mode.

4.3.8 The rear-panel GPIB switch bank provides a "Talk-Only" selector switch (see Subsection 4.6.2).

4.3.9 The 1994 is preset at GPIB address 03 when shipped.

4.4 GPIB FUNCTIONAL CHECK

4.4.1 Introduction

4.4.1.1 The following procedure verifies the 1994's capability to accept, process, and transmit GPIB messages. Complete a satisfactory check of the counter under local control before starting this procedure (see Subsection 2.9).

4.4.1.2 Successful completion of the GPIB check indicates that the counter's GPIB interface is operating properly.

4.4.1.3 For recommended test equipment use a Hewlett-Packard Model HP-85 GPIB controller with I/O ROM in a drawer. It is assumed that the select code for the controller I/O port is 7 and the GPIB address of the counter is 15.

NOTE:

If any other controller or selected/GPIB address combination is used, the GPIB commands in the following procedure will require change.

4.4.1.4 Connect the controller to the GPIB interface of the counter using a standard GPIB cable. No connection should be made to Inputs A, B, or C.

4.4.2 Remote and Local Check

4.4.2.1 Now perform the following procedure:

a. Power-on the counter. Verify that the REM, ADDR, and SRQ LEDs flash on and off once. If the indicators do not flash or flash continuously, there is a fault on the GPIB PCB.

b. Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command true, together with the 1994's listen address	REMOTE 715	

c. Verify that the REM LED lights

d. Test as shown below:

Action	HP-85 Code	Your Controller
Send the device-dependent command CK	OUTPUT 715; "CK"	

e. Verify that the ADDR LED lights and that the Check mode is selected

f. Test as shown below:

Action	HP-85 Code	Your Controller
Send the 1994's listen address followed by the GTL command	LOCAL 715	

g. Verify that the REM LED is off. The ADDR LED will also extinguish if the controller automatically transmits the UNL (unlisten) command true as with the HP-85

4.4.3 Local Lockout and Clear Lockout Check

4.4.3.1 Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command true, together with the 1994's listen address	REMOTE 715	
Send the LLO command	LOCAL LOCKOUT 7	

a. Verify that the REM LED lights. Operate the LOCAL key on the front panel and check that the REM LED remains lit

b. Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command false	LOCAL 7	

c. Verify that the REM LED is off

d. Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command true, together with the 1994's listen address	REMOTE 715	

e. Verify that the REM LED lights. Operate the LOCAL key and check that the REM LED extinguishes

4.4.4 Data Output Check

4.4.4.1 Test as shown below:

Action	HP-85 Code	Your Controller
Send the 1994 in the Check mode by sending the counter's listen address, followed by the device-dependent command CK	OUTPUT 715; "CK"	
Prepare a store to receive a 21-byte data string	DIM Z$ 21	
Send the 1994's talk address. Store the 21-byte data string in the prepared store	ENTER 715; Z$	
Display the contents of the store	DISP 7$	

a. Verify that the HP-85 display reads CK+0010.0000000E+06 with the cursor moved to the next line, indicating that carriage return (CR) and line feed (LF) have been accepted

4.4.5 SRQ and Status Byte Check

4.4.5.1 Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command true	REMOTE 7	
Set the 1994 to transmit the SRQ command when an error is detected, and force the generation of error code 0_ by sending device-dependent command XXX	OUTPUT 715; "IPXXX"	
Store the status of the GPIB interface of the controller, in binary form, as variable T	STATUS 7,2; T	
Display the status of the SRQ line	DISP "SRQ="; BIT (T,5)	

a. Verify that the HP-85 display reads SRQ=1, the SRQ status bit is at logic 1. Confirm that the SRQ LED is lit

b. Test as shown below:

Action	HP-85 Code	Your Controller
Conduct a serial poll and store the status byte as variable R	R=SPOLL (715)	
Display variable R	DISP "R="; R	

c. Verify that the SRQ LED is extinguished when the serial poll is made. The value of R should be 101 (in binary form, R should be 0000000001100101)

4.4.6 Device Clear and Selected Device Clear Check

4.4.6.1 Test as shown below:

Action	HP-85 Code	Your Controller
Set the 1994 to the Total A by B mode by sending the instrument's listen address, followed by device-dependent command TA	OUTPUT 715; "TA"	
Send the DCL command true	CLEAR 7	

a. Verify that the function indicated on the front panel changes to FREQ A

b. Test as shown below:

Action	HP-85 Code	Your Controller
Reset the 1994 to the Total A by B mode by sending the instrument's listen address, followed by device-dependent command TA	OUTPUT 715; "TA"	
Send the SDC message true	CLEAR 715	

c. Verify that the function indicated on the front panel changes to FREQ A

4.4.7 IFC Check

4.4.7.1 Test as shown below:

Action	HP-85 Code	Your Controller
Send the ATN message false	RESUME 7	
Send the IFC message true	ABORTIO 7	

a. Verify that the ADDR LED is extinguished

4.4.8 Talk-Only Selector Check

4.4.8.1 Perform the following procedure:

a. Set the Talk-Only switch on the 1994's rear panel to 1. Verify that the REM LED is turned off and the ADDR LED lights

b. Set the Talk-Only switch to 0. Verify that the ADDR LED is turned off

4.5 INTERFACE MESSAGE REPERTOIRE and RESPONSE

4.5.1 Introduction

4.5.1.1 The 1994 is equipped with a standard GPIB interface designed to meet IEEE-STD-488-1978 specifications. These specifications provide a definition of multiline interface messages, dividing them into two main groups:

a. Primary command group

b. Secondary command group

This counter includes only the primary commands in its interface repertoire.

4.5.1.2 The primary command group is further divided into four categories:

a. Listen address commands

b. Talk address commands

c. Addressed commands

d. Universal commands

4.5.2 Listen and Talk Address Commands

4.5.2.1 The counter responds to address messages defined by the programmed GPIB address set from the rear panel. Refer back to Table 4.2 as required for a listing of the 31 talk and 31 listen addresses. The 1994 will respond to talk and listen address messages regardless of its addressed state.

4.5.2.2 Listen Addresses

4.5.2.2.1 Receipt by the counter of a listen address makes it a listener. If previously addressed to talk, the counter ceases to be a talker. In in Local mode, the counter reverts to its Remote state, provided the REN message is true.

4.5.2.3 Talk Addresses

4.5.2.3.1 Receipt by the counter of a talk address makes it a talker. If previously addressed to listen, the counter ceases to be a listener. If in Local mode, the counter will remain under local control.

4.5.2.4 Talk Addresses - Other Devices

4.5.2.4.1 If the counter was previously addressed to talk, then receives the talk address of another bus device, the 1994 ceases to be a talker.

4.5.3 Addressed and Universal Commands

4.5.3.1 Table 4.3 lists the Addressed and Universal commands to which the 1994 responds. These interface commands are recognized because they are sent with the ATN message as true. The following paragraphs describe the counter's response to each of these commands.

Table 4.3 - Addressed and Universal Commands

Message	Meaning	Hex Code	Decimal Equivalent	Data Line Code						
				7	6	5	4	3	2	1
GTL	Go To Local	01	1	0	0	0	0	0	0	1
SDC	Selected Device Clear	04	4	0	0	0	0	1	0	0
GET	Group Execute Trigger	08	8	0	0	0	1	0	0	0
LLO	Local Lock Out	11	17	0	0	1	0	0	0	1
DCL	Device Clear	14	10	0	0	1	0	1	0	0
SPE	Serial Poll Enable	18	24	0	0	1	1	0	0	0
SPD	Serial Poll Disable	19	25	0	0	1	1	0	0	1
UNL	Unlisten	3F	63	0	1	1	1	1	1	1
UNT	Untalk	5F	9	1	0	1	1	1	1	1

4.5.3.2 Go To Local (GTL)

4.5.3.2.1 Provided the counter is in remote and a listener, it reverts to local operation. The counter remains addressed to listen. It now operates by front-panel controls, until returned to remote control by receipt of the first byte of a device-dependent message. The decimal and hex equivalents are both 01.

4.5.3.3 Selected Device Clear (SDC)

4.5.3.3.1 Provided the counter is in remote and a listener, it reverts to home state. The condition of the GPIB interface remains unchanged. The decimal and hex equivalents are both 04.

4.5.3.4 Group Execute Trigger (GET)

4.5.3.4.1 Provided the counter is a listener and no measurement is in progress, it triggers a previously programmed measurement. The GET command permits several bus devices to simultaneously perform a number of different operations. (All bus members have been previously programmed to perform a function on receiving the GET command or trigger command.) The decimal and hex equivalents are both 08.

4.5.3.5 Local Lockout (LLO)

4.5.3.5.1 The counter responds to the LLO command regardless of its addressed state. The LLO command disables the LOCAL key on the front panel. Local lockout is cleared by sending the REN message as false, returning all bus devices to the local control state. A GTL command returns the counter to local control. The decimal and hex equivalents are 17 and 11, respectively.

4.5.3.6 Device Clear (DCL)

4.5.3.6.1 Same as the SDC command, except that all bus devices in remote are cleared. The counter responds to this command regardless of its addressed state. The decimal and hex equivalents are 10 and 14, respectively.

4.5.3.7 Serial Poll Enable (SPE)

4.5.3.7.1 This command permits all bus members, including the counter, to set their SRQ line to binary 1, informing the controller that attention is required. The 1994 responds to this command regardless of its addressed state. Each bus member, having been made a talker, is then serially interrogated by the controller to determine which bus member(s) requested service and the purpose of each request. Bus members respond by transmitting their respective status bytes to the controller. All members respond to the SPE regardless of their addressed state. The hex and decimal equivalents are 18 and 24, respectively.

4.5.3.8 Serial Poll Disable (SPD)

4.5.3.8.1 This command returns all bus members to normal operation after completion of a serial poll. All bus members respond to the SPD command regardless of their addressed state. If addressed to talk, a bus device will put its data output string on the GPIB, provided such data is available in its output buffer. The decimal and hex equivalents are 25 and 19, respectively.

4.5.3.9 Untalk (UNT)

4.5.3.9.1 This universal command instructs all talkers, including the counter, to return to their untalk or talker-idle state. All bus members are also removed from their talker state whenever a talk address other than their own is received. In the Untalk state, the front-panel ADDR LED is turned off. The decimal and hex equivalents are 9 and 5F, respectively.

4.5.3.10 Unlisten (UNL)

4.5.3.10.1 This universal command instructs all listeners, including the counter, to return to their unlisten or listen-idle state. In the Unlisten state, the front-panel ADDR LED is turned off. The decimal and hex equivalents are 63 and 3F, respectively.

4.6 GPIB OPERATING MODES

4.6.1 Introduction

4.6.1.1 Before operating the counter on the GPIB, ensure that the instrument has been assigned its correct bus address (see Subsection 4.3) and that the correct AC line voltage has been selected (see Subsection 2.7.2). The last instruction is especially important if the 1994 is being used for the first time or at a new location.

4.6.1.2 The 1994 can be operated on the GPIB in either its Talk-Only or Addressed mode.

4.6.2 Talk-Only Mode

4.6.2.1 To set the counter in this mode, place the "Talk Only" switch of the GPIB switch bank in its logic "1" position. The GPIB interface is now in the Talk-Only mode and the settings of switches A1 to A5 are irrelevant.

4.6.2.2 The Talk-Only mode may be used in systems not having a controller. Such a system permits remote reading of counter measurement data, however, the instrument is controlled from the front panel (see Section 3).

4.6.2.3 The counter determines the rate at which measurements are made. The output buffer is updated at the end of each measurement cycle, overwriting the previous measurement data if not transferred to the listener.

4.6.2.4 The listener triggers the transfer to data from the counter. The counter's output buffer is cleared when data transfer is completed.

4.6.2.5 Differences between the measurement rate and data transfer trigger rate are resolved as follows:

a. If data transfer is in progress at the end of a measurement cycle, updating of the output buffer is delayed. Data transferred will correspond to the previous measurement cycle

b. If data transfer is requested during a measurement cycle and the output buffer is empty, data transfer is delayed until the buffer is updated. Data transferred will then correspond to the latest measurement cycle

c. If a measurement cycle is completed before the results of the previous cycle have commenced transfer to the listener, the buffer will be updated. The data from the previous cycle will be overwritten and lost.

4.6.2.6 Measurement rate in the 1994 is affected by the following:

a. The gate time can be controlled by selecting an appropriate display resolution or setting a specific gate time

b. A time interval delay can be set using the range of 200 µs to 99.9 s

c. The counter can be operated in the Hold mode (single-shot measurements). Readings are displayed indefinitely in Hold while the RESET key is pressed, initiating a new measurement cycle

4.6.3 Addressed Mode

4.6.3.1 In the Addressed mode, all of the counter's functions (except POWER ON/OFF and STBY) can be controlled by device-dependent commands (see Subsection 4.10). These commands are sent over the GPIB after the counter has been addressed to listen. Completed measurement readings and counter status information are then read back over the bus after the counter is addressed to talk. If the counter is addressed to talk when its output buffer is empty, no data transfer will occur and bus activity will cease. Data transfer will start again after the output buffer is updated at the completion of the next measurement cycle.

4.7 OUTPUT MESSAGE FORMAT (TALKER)

4.7.1 Introduction

4.7.1.1 Refer to Table 4.4. The same output format is used for transmitting measurement values as well as numbers recalled from the counter's internal stores.

4.7.1.2 The output message consists of a string of 21 ASCII characters for each transmitted value. Measurement units should be assumed as hertz, seconds, volts, degrees, or a ratio, depending on commands previously sent to the counter.

NOTE:

An SRQ message is not enabled by data recall from the counter's stores.

Table 4.4 – Output Message Format

Byte No.	Interpretation	Permitted ASCII Characters	Notes
1	Function letter or space-the latter only if programmed by special function	See Table 4.5	Spaces are transmitted
2	Function letter or space	See Table 4.5	
3	Measurement sign	+ or -	
4	Most significant digit	0 to 9	Bytes 4 to 15 will always include 11 digits and decimal point. Zeros are added when necessary in the more significant positions
5	Digit 0 to 9 or .	↓	
6	↓	↓	
7	↓	↓	
8	↓	↓	
9	↓	↓	
10	↓	↓	
11	↓	↓	
12	↓	↓	
13	↓	↓	
14	↓	↓	
15	Least significant digit	↓	
16	Exponent indicator	E	Upper case only
17	Exponent sign	+ or -	
18	More significant digit	0 to 9	Exponent is a multiple of 3
19	Less significant digit	0 to 9	
20	Carriage return	CR	
21	Line feed	LF	

Table 4.5 - Function Letters

Function/Operation	Function Letters
Frequency A	FA
Frequency B	FB
Frequency C	FC
Period A	PA
Time Interval A→B	TI
Totalize A by B	TA
Ratio A/B	RA
Ratio C/B	RC
Rise Time A	RT
Fall Time A	FT
Positive Pulse Width A	PW
Negative Pulse Width A	NW
Phase A rel B	PH
Recalled Data	**Function Letters**
Unit Type	UT
Resolution	RS
Trigger Level A	LA
Trigger Level B	LB
Math Constant X	MX
Math Constant Y	MY
Math Constant Z	MZ
Delay Time	DT
Special Function	SF
Master Software Issue	MS
GPIB Software Issue	GS
Gate Time	GT
Memory (Non-Vol)	M

4.7.2 High-Speed Data Output Mode

4.7.2.1 The 1994 provides a High Speed Output mode which is capable of transmitting over 150 readings per second in raw data format. The High Speed Output mode is intended for applications in which the controller can store the readings for later processing. Once the data is received, it must be processed to extract useful information.

4.7.2.2 Table 4.6 below shows the format of the data sent by the 1994 while in the High Speed Output mode. An explanation of symbols follows the table.

Table 4.6 – High Speed Output Mode Format

Byte No.	D7	D6	D5	D4	D3	D2	D1	D0	Comments
1	E7	E6	E5	E4	E3	E2	E1	E0	Least significant byte of Event counter
2	E15	E14	E13	E12	E11	E10	E9	E8	Next to least significant byte of Event counter
3	E23	E22	E21	E20	E19	E18	E17	E16	Next most significant byte of Event counter
4	—	T26	T25	T24	—	E26	E25	E24	Most significant three bits of Time and Event counters
5	T7	T6	T5	T4	T3	T2	T1	T0	Least significant byte of Time counter
6	T15	T14	T13	T12	T11	T10	T9	T8	Next to least significant byte of Time counter
7	T23	T22	T21	T20	T19	T18	T17	T16	Next most significant byte of Time counter
8	TT7	TT6	TT5	TT4	TT3	TT2	TT1	TT0	Least significant byte of Start TEC counter
9	TP11	TP10	TP9	TP8	TT11	TT10	TT9	TT8	Most significant four bits of Start TEC and Stop TEC counters
10	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0	Least significant byte of Stop TEC counter
11	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	Least significant byte of short calibration Start TEC counter
12	SP11	SP10	SP9	SP8	ST11	ST10	ST9	ST8	Most significant four bits of short calibration Start TEC and Stop TEC counters
13	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Least significant byte of short calibration Stop TEC counter
14	LT7	LT6	LT5	LT4	LT3	LT2	LT1	LT0	Least significant byte of long calibration Start TEC counter

Table 4.6 - High Speed Output Mode Format (Cont'd)

Byte No.	D7	D6	D5	D4	D3	D2	D1	D0	Comments
15	LP11	LP10	LP9	LP8	LT11	LT10	LT9	LT8	Most significant four bits of long calibration Start TEC and Stop TEC counters
16	LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0	Least significant byte of long calibration Stop TEC counters
17	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	Least significant byte of delay calibration Start TEC counter
18	DP11	DP10	DP9	DP8	DT11	DT10	DT9	DT8	Most significant four bits of delay calibration Start TEC and Stop TEC counters
19	DP7	DP6	DP5	DP4	DP3	DP2	DP1	DP0	Least significant byte of delay calibration Stop TEC counter

4.7.2.3 The Event and Time counters are 24-bit binary numbers while each of the TEC counters are 12-bit binary numbers. The following symbols will be used to describe each of the counters:

Symbol	Description
E	Event counter
T	Time counter
TT	TEC Start counter
TP	TEC Stop counter
ST	Short calibration TEC Start counter
SP	Short calibration TEC Stop counter
LT	Long calibration TEC Start counter
LP	Long calibration TEC Stop counter
DT	Delay calibration TEC Start counter
DP	Delay calibration TEC Stop counter

4.7.2.4 In order to calculate the measurement, the following formulas must be used:

a. FREQUENCY = E/(corrected time)

b. PERIOD = (corrected time)/E

c. TIME INTERVAL = corrected delay time

d. FREQUENCY RATIO = E/T

where:

corrected time = T + ((TT-ST)/(LT-ST) - (TP-SP)/(LP-SP))

corrected delay time = T + ((TT-ST)/(LT-ST) - (TP-SP)/(DP-SP))

4.7.2.5 Below is a program example for frequency measurement (using a Hewlett-Packard Model 9825A controller). For other measurement functions, substitute the formulas mentioned in par. 4.7.2.4 in line 20 of the program.

```
 0: dim A[150]
 1: buf "in",100,
  3
 2: wrt 700,"fa"
 3: wrt 700,"fe"
 4: tfr 700,"in",
  19
 5: if rds("in")<
  0;jmp 0
 6: for I=1 to 19
 7: rdb("in")→A[I
  ]
 8: next I
 9: wrt 700,"fd"
10: A[9]mod16*
  256+A[8]→T
11: A[9]/16mod16
  *256+A[10]→P
12: A[12]mod16*
  256+A[11]→U
13: A[12]/16mod1
  6*256+A[13]→Q
14: A[15]mod16*
  256+A[14]→V
15: A[15]/16mod1
  6*256+A[16]→R
16: A[18]mod16*
  256+A[17]→W
17: A[18]/16mod1
  6*256+A[19]→S
18: ((A[4]mod16*
  256+A[3])*256+
  A[2])*256+A[1]→
  C
19: ((A[4]/16mod
  8*256+A[7])*.
  256+A[6])*256+
  A[5]→E
20: (T-U)/(V-U)-
  (P-Q)/(R-Q)→F
21: flt 7
22: dsp C*2/((E+
  F)*1e-7),R-Q
23: sto 3
*11737
```

4.8 SERVICE REQUEST (SRQ)

4.8.1 The counter can be set, by means of device-dependent commands to enable an SRQ message whenever:

a. A measurement cycle is completed

b. A change of frequency standard occurs

c. An error state is detected

d. Any combination of a, b, and c

4.8.2 SRQ enablement may be inhibited. Refer to Table 4.18 which provides the necessary SRQ commands. When in home state, condition "c" indicated above is active.

NOTE:

An SRQ message is not enabled by data recall from the counter's stores.

4.9 STATUS BYTE

4.9.1 To inform the controller of its status, the counter assembles and transmits a status message referred to as a status byte. The controller generates a serial poll enable cycle to determine which bus member has requested service and the purpose of the request. When the 1994 receives the SPE command, and has been made a talker, it outputs the status byte to the controller. Table 4.7 shows the format of the counter's status byte.

Table 4.7 - Status Byte Format

DIO Line	Function
1	Error - Least significant bit - See NOTE 1
2	Codes
3	in Binary - Most significant bit
4	1 = Frequency standard changed
5	1 = Reading ready - See NOTE 2
6	1 = Error condition
7	1 = Service requested
8	1 = Gate open

Table 4.7 - Status Byte Format (Cont'd)

DIO Line	Function
	NOTE 1: The error codes and numbers are as follows: 1 = Phase measurement attempted on waveforms of differing frequency (Ratio ≠ 1) 2 = Result out-of-range of display 3 = Overflow of internal counters 4 = Numerical entry error 5 = GPIB syntax (programming) error } See NOTE 3 No measurement output string is available if error codes 1, 2, or 3 is produced. **NOTE 2:** Regardless of the current SRQ mode, the SRQ message that a reading is ready is not generated after a data-recall operation. **NOTE 3:** The five error codes are cleared as follows: Error 1 - correct the difference in input frequencies or change the measurement mode Error 2 - complete an in-range measurement Error 3 - complete an in-range measurement Error 4 - complete a valid numerical entry Error 5 - the erroneous command string will be correctly executed up to the error; the rest will be handshaken, but not executed. Receipt of the next valid command clears the error

4.10 INPUT COMMANDS (LISTENER)

4.10.1 Introduction

4.10.1.1 The 1994 responds to device-dependent commands in a "deferred" mode. This means that the GPIB interface continues to accept commands until a terminating character or message is received, then the entire string will be executed. There is no "immediate" mode in which commands are obeyed as they are received.

4.10.2 Device-Dependent Commands

4.10.2.1 When the counter is addressed to listen, it can be controlled by device-dependent commands. These commands are listed below, and tabulated in Tables 4.9 to 4.19.

a. Table 4.9 - Instrument Preset Code
b. Table 4.10 - Numerical Input Format
c. Table 4.11 - Measurement Function Codes
d. Table 4.12 - Numerical Input Ranges
e. Table 4.13 - Resolution Selection
f. Table 4.14 - Input Control Codes
g. Table 4.15 - Measurement Control Codes
h. Table 4.16 - Store and Recall Codes
i. Table 4.17 - Special Function Codes
j. Table 4.18 - Service Request Codes
k. Table 4.19 - Alphabetic List of Command Codes

4.10.2.2 Device-dependent commands are executed sequentially beginning with the first one sent and ending with the last.

4.10.2.3 If more than one command is to be sent, no delimiters are required. If necessary, commas, spaces, and semicolons may be included in the command strings for clarification without affecting counter operation.

4.10.2.4 Each command string must be followed by an end-of-string terminating group. Table 4.8 shows the valid terminator groups.

Table 4. 8 - Permitted Terminators

1	2	3	4	5	6
LF	LF EOI	CR EOI	CR LF	CR LF EOI	Last Character EOI

Where LF=Line feed, CR=carriage return; EOI is considered true

4.10.2.5 Table 4.9 provides the instrument preset code for the 1994.

Table 4.9 - Instrument Preset Code

Function	Code
Sets counter functions and settings to home state	IP

4.10.2.6 Some of the device-dependent commands in the following tables require additional numerical input data. Such numerical input succeeds its command and is indicated by an asterisk (*) in the tabulations. Also, home-states are underlined. Refer to Table 4.10 as required for numerical input format.

Table 4.10 - Numerical Input Format

Byte No.	Interpretation	Permitted ASCII Characters
1	Sign of mantissa	+ or -
2	Most significant digit	0 to 9 or .
3	Digit	↓
4	↓	
5		
6		
7		
8		
9		
10		
11	Least significant digit	
12	Exponent indicator	E or e
13	Exponent sign/space	+ or - or space
14	More significant digit	0 to 9
15	Less significant digit	0 to 9

NOTE 1:

Spaces, nulls, or zeros occurring before byte 1 are ignored by the counter.

NOTE 2:

Byte 1 may be omitted and a positive mantissa assumed.

NOTE 3:

Bytes 2 to 11 may have up to 9 digits and a decimal point. The decimal point, however, is not essential. After entry of 9 digits (without a decimal point), additional digits are ignored and a GPIB programming error is generated. Excess digits that are truncated will still increase the power-of-ten stored. Also, if fewer than 9 digits are needed, unused bytes may be omitted.

NOTE 4:

Spaces or nulls entered between bytes 11 and 12 are ignored by the counter.

NOTE 5:

Bytes 12 to 15 (exponent group) may be omitted. Also, byte 13 may be omitted or transmitted as a space (a positive exponent should be assumed in either instance).

NOTE 6:

Byte 15 may be omitted for a single-digit exponent.

Table 4.10 - Numerical Input Format (Cont'd)

Byte No.	Interpretation	Permitted ASCII Characters
	NOTE 7:	
Numbers may be terminated by one of the same terminators used for output messages, or by another device-dependent message.		
	NOTE 8:	
Units are implied; volts for trigger levels, seconds for gate/delay times.		

4.10.2.7 Table 4.11 presents the measurement function codes for the 1994.

Table 4.11 - Measurement Function Codes

Function	Code
Frequency A	FA
Frequency B	FB
Frequency C	FC
Period A	PA
Time Interval A→B	TI
Totalize A by B	TA
Ratio A/B	RA
Ratio C/B	RC
Rise Time A	RT
Fall Time A	FT
Positive Pulse Width A	PW
Negative Pulse Width A	NW
Phase A rel B	PH
Check	CK

NOTE:

Option 41 must be installed in the 1994 for FC and RC to be accepted as valid commands.

4.10.2.8 Table 4.12 provides the various numerical input ranges for the 1994.

Table 4.12 - Numerical Input Ranges

Function	Command Code	Numerical Limits	
		Low	High
Resolution	SRS	3	10
Trigger Level (X1)	SLA, SLB	-5.1	+5.1
Trigger Level (X10)	SLA, SLB	-51	+51
Math Constant	SMX, SMY, SMZ	$\geq 1 \times 10^{-9}$	$< 1 \times 10^{10}$
		0	
		$> -1 \times 10^{10}$	$\leq -1 \times 10^{-9}$
Delay/Gate Time	SDT/SGT	$\geq 200\ \mu s$	$\leq 99.999\ s$
Non-Volatile Memory	SM/RM	≥ 0	≤ 9

NOTE 1:

Entered numbers will be rounded up before storage as follows:

a. Trigger level X1 to next multiple of 20 mV

b. Trigger level X10 to next multiple of 200 mV

c. Delay/gate time to next multiple of 25.6 µs

NOTE 2:

Resolution entries are rounded down to the next integer. Refer to Table 3.12 for related gate times and GPIB resolution numbers.

NOTE 3:

Math constant Z can be set to zero. However, an error message will result if the Math function is enabled with this value set.

NOTE 4:

Non-Volatile Memory commands require a single-digit suffix ranging from 0 to 9.

4.10.2.9 Table 4.13 provides the 1994 GPIB resolution selection.

Table 4.13 - Resolution Selection

GPIB Resolution Number	Number of Selected, Digits in Frequency, Period, Ratio, and Check	Gate Time
10	9 + Overflow	10 s
9	9	1 s
8	8	100 ms
7	7	10 ms
6	6	1 ms
5	5	1 ms
4	4	1 ms
3	3	1 ms

NOTE:

Refer to Table 3.12 as required. It shows the relationship of gate time and display resolution in the 1994.

4.10.2.10 The following tables complete the necessary GPIB commands for the 1994:

Table 4.14 - Input Control Codes

Function	Code
FILTER Disable/Enable	AFD/AFE
COM A Disable/Enable	BCS/BCC
DC/AC Coupling A	ADC/AAC
DC/AC Coupling B	BDC/BAC
1 MΩ/50Ω impedance A	AHI/ALI
1 MΩ/50Ω impedance B	BHI/BLI
Slope A +ve/-ve	APS/ANS
Slope B +ve/-ve	BPS/BNS
X10 attenuator A Disable/Enable	AAD/AAE
X10 attenuator B Disable/Enable	BAD/BAE
Manual/AUTO-TRIG A	AMN/AAU
Manual/AUTO-TRIG B	BMN/BAU

Table 4.15 - Measurement Control Codes

Function	Code
Continuous measurement mode selection	T0 (See NOTE 1)
Single (One-Shot) measurement mode selection	T1 (See NOTE 2)
Start Totalize or trigger a measurement (T1 mode)	T2 (See NOTE 3)
Stop Totalize	T3 (See NOTE 3)
Read current value while measurement is in progress (i.e., next reading on the fly)	RF (See NOTE 4)
Math function Disable/Enable	MD/ME
Delay Disable/Enable	DD/DE
100 AVG Disable/Enable	NA/AE
Fast data output Disable/Enable	FD/FE
Reset measurement	RE

NOTE 1:

In continuous measurement mode, the output buffer is updated at the end of each gate period. If the buffer is being read out via the bus when the gate period ends, updating is delayed until reading is complete.

NOTE 2:

In single-measurement mode, the output buffer is cleared every time a T1 command is received. The measurement completed must be read, therefore, before the next measurement cycle is triggered.

NOTE 3:

In making totalize measurements, T2 and T3 commands are used with the TA command and Special Function 61. In this mode, the readings executed in successive totalize periods are cumulative; (the RE command being used to reset the count to zero when required).

NOTE 4:

The RF command must be sent each time a reading is required. The reading is obtained when the counter is made a talker.

Table 4.16 - Store and Recall Codes

Function	Code
Recall unit type	RUT
Store/Recall display resolution (Defaults to 8)	*SRS/RRS
Store/Recall trigger level A (Defaults to 0V)	*SLA/RLA (See NOTE 1)
Store/Recall trigger level B (Defaults to 0V)	*SLB/RLB (See NOTE 1)
Store/Recall math constant X (Defaults to 0)	*SMX/RMX
Store/Recall math constant Y (Defaults to 1)	*SMY/RMY
Store/Recall math constant Z (Defaults to 1)	*SMZ/RMZ
Store/Recall arming delay time (Defaults to 200 μs)	*SDT/RDT
Store/Recall gate time (Defaults to 100 ms)	*SGT/RGT
Store/Recall memory (0 through 9)	*SM/RM (See NOTE 2)
Recall special function (Defaults to all SFs off)	RSF
Recall master software issue	RMS
Recall GPIB software issue	RGS

NOTE 1:

The manual trigger level is automatically scaled by a factor of 10 when the X10 attenuator key is toggled in or out-of-circuit. The correct input attenuation must be selected before storing or recalling the trigger level.

NOTE 2:

The SM and RM codes are used to store and recall complete measurement setups. Both SM and RM must be followed by a measurement setup number from 0 to 9.

Table 4.17 - Special Function Codes

Function	Code
Special functions Disabled/Enabled	SFD/SFE
Store special function nn	Snn

NOTE 1:

The list of special functions (SFs) is provided in Table 3.13.

NOTE 2:

Storing a special function when special functions are enabled immediately enables that special function.

Table 4.18 - Service Request Codes

Function	Code
SRQ generation inhibited	Q0
SRQ generation inhibited upon error detected	Q1
SRQ generation inhibited for measurement ready	Q2
SRQ generation inhibited for measurement ready or error detected	Q3
SRQ generation inhibited for frequency standard changed (internal to external/or external to internal)	04
SRQ generation inhibited for frequency standard change or error detection	Q5
SRQ generation inhibited for measurement ready or frequency standard change	Q6
SRQ generation inhibited for measurement ready, frequency standard changed, or error detected (internal to external or external to internal)	Q7

NOTE:

An SRQ message is not generated by data recalled from stores.

Table 4.19 - Alphabetic List of Command Codes

Code	Command	Code	Command
AAC	A Channel, AC coupling	NA	100 Average disabled
AAD	A Channel, X10 attenuator disabled	NW	Negative pulse width A
		PA	Period A
AAE	A Channel, X10 attenuator enabled	PH	Phase A relative to B
		PW	Positive pulse width A
AAU	A Channel auto-trigger	Qn	SRQ mode
ADC	A Channel, DC coupling	RA	Ratio A/B
AE	100 Average enabled	RC	Ratio C/B
AFD	A Channel filter disabled	RDT	Recall arming delay time
AFE	A Channel filter enabled	RE	Reset measurement
AHI	A Channel, 1 Mohm	RF	Read total so far
ALI	A Channel, 50 ohms	RGS	Recall GPIB software issue number
AMN	A Channel manual trigger		
ANS	A Channel, -ve slope	RGT	Recall gate time
APS	A Channel, +ve slope	RLA	Recall trigger level A
BAC	B Channel, AC coupling	RLB	Recall trigger level B
BAD	B Channel, X10 attenuator disabled	RM	Recall Non-Volatile Memory
		RMS	Recall master software issue number
BAE	B Channel, X10 attenuator enabled		
		RMX	Recall math constant X
		RMY	Recall math constant Y

Table 4.19 - Alphabetic List of Command Codes (Cont'd)

Code	Command	Code	Command
BAU	B Channel auto-trigger	RMZ	Recall math constant Z
BCC	A and B Channels common	RRS	Recall display resolution
BCS	A and B Channels separate	RSF	Recall special function
BDC	B Channel, DC coupling	RT	Rise time A
BHI	B Channel, 1 Mohm	RUT	Recall unit type
BLI	B Channel, 50 ohms	Snn	Special function number
BMN	B Channel manual trigger	SDT	Store arming delay time
BNS	B Channel, -ve slope	SFD	Special function disabled
BPS	B Channel, +ve slope	SFE	Special function enabled
CK	Check	SGT	Store gate time
DD	Delay disabled	SLA	Store trigger level A
DE	Delay enabled	SLB	Store trigger level B
FA	Frequency A	SM	Store Non-Volatile Memory
FB	Frequency B	SMX	Store math constant X
FC	Frequency C	SMY	Store math constant Y
FD	Fast data output disabled	SMZ	Store math constant Z
FE	Fast data output enabled	SRS	Store display resolution
FT	Fall time A	Tn	Measurement mode or start/stop reading
IP	Instrument Preset		
MD	Math function disabled	TA	Total A by B
ME	Math function enabled	TI	Time Interval

SECTION 5 GENERAL THEORY OF OPERATION

5.1 INTRODUCTION

5.1.1 This section describes the general theory of operation for the 1994.

5.1.2 The theory of operation provided is based on the simplified overall block diagram shown in Figure 5.1. Key circuit blocks of the 1994 are described and supported in this section using simplified block and schematic diagrams. These diagrams supplement the complete schematics found in Section 7 of this manual. As much as possible, the simplified schematic and block diagrams provided here are annotated with the same reference designators found in the complete schematics. This should facilitate cross-referencing between this section of the manual and the schematics.

5.1.3 Integrated circuits (ICs) in the following circuit descriptions are designated by circuit references provided on the supporting simplified block and schematic diagrams. The IC designations employed in the following key circuit descriptions follow those found in supplied schematics.

When an IC package contains more than one circuit, suffix letters are used to distinguish them (e.g., IC1a). Finally, when it is necessary to identify a specific pin in an IC, the reference designator, with a suffix letter if necessary, is followed by a hyphen and then the required pin number (e.g., IC1a-1).

5.2 FUNCTIONAL BLOCKS

5.2.1 The 1994 contains the following ten main functional blocks:

a. Channel A/B block (see Subsection 5.3.1)

b. Channel C block (see Subsection 5.3.2)

c. Measurement block (see Subsection 5.3.3)

d. Display block (see Subsection 5.3.4)

e. Keyboard block (see Subsection 5.3.5)

f. Microprocessor block (see Subsection 5.3.6)

g. Standby and IRQ block (see Subsection 5.3.7)

h. Power Supply block (see Subsection 5.3.8)

i. Internal Frequency Standard block (see Subsection 5.3.9)

j. GPIB Interface (see Subsection 5.3.10)

5.2.2 The functional relationship between the blocks of the 1994 is illustrated in Figure 5.1. The measurement block is internally configured by the microprocessor according to the instructions entered via the keyboard or over the GPIB. The signal to be measured and the signal from the frequency standard are fed to the measurement block. The measured result is passed to the microprocessor. If mathematical manipulation of the result is required, this is performed by the microprocessor before the final output is passed to the display or system.

5.2.3 The standby and IRQ block handles instructions to switch to standby. These instructions are received from the keyboard block and interrupt requests made by other systems.

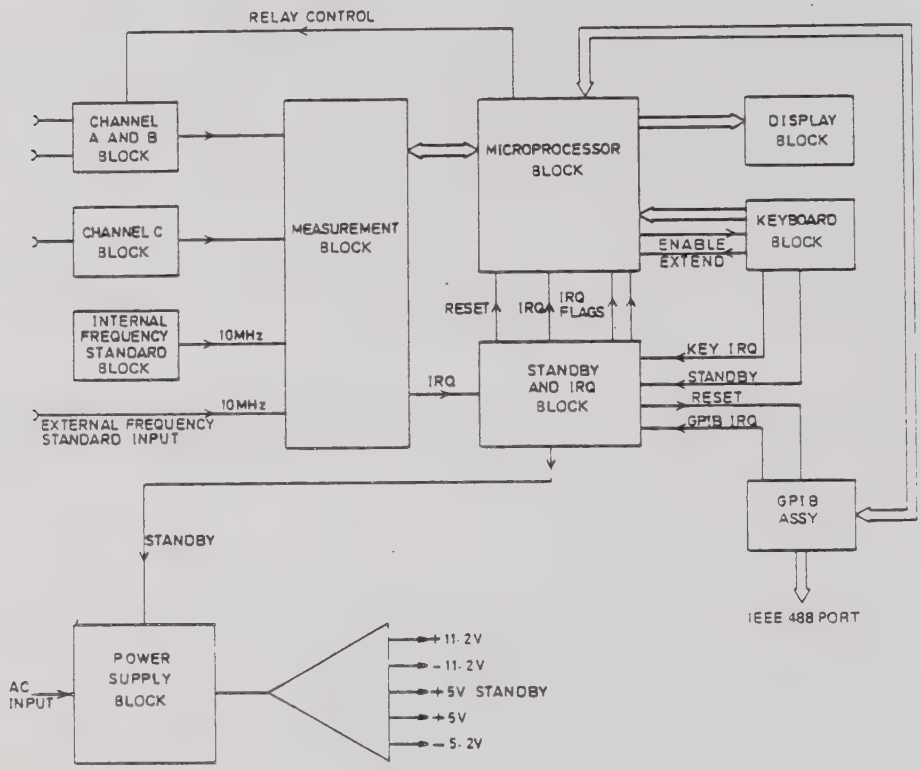


Figure 5.1 - Simplified Overall Block Diagram

5.3 THEORY OF OPERATION BY BLOCK

5.3.1 Channel A/B Block

5.3.1.1 Functional Description

5.3.1.1.1 Channel A/B block processes the signals applied at the respective A/B inputs to produce differential pairs of signals which are fed to the measurement block. A block diagram is shown in Figure 5.2.

5.3.1.1.2 Each channel includes relay-controlled circuits which allow selection of 50Ω /1MΩ input impedance, AC/DC coupling, and x1/x10 attenuation. The COM(mon) A configuration (Channel B signal disconnected and Channel A signal connected to both amplifiers in parallel) can be selected.

5.3.1.1.3 The channel amplifiers feature separate high frequency and low frequency paths. The crossover frequency is nominally 5 kHz. Signal filtering can be introduced, in Channel A only, by disconnecting the high-frequency amplifier path and increasing the bandwidth of the low frequency path to 50 kHz nominal. The signals from the high and low frequency paths are combined and drive a Schmitt trigger output stage.

5.3.1.1.4 The trigger levels for the two channels are derived independently in the digital-to-analog converter (DAC) using data supplied from the microprocessor.

5.3.1.1.5 Control signals for the system relays are supplied from the microprocessor.

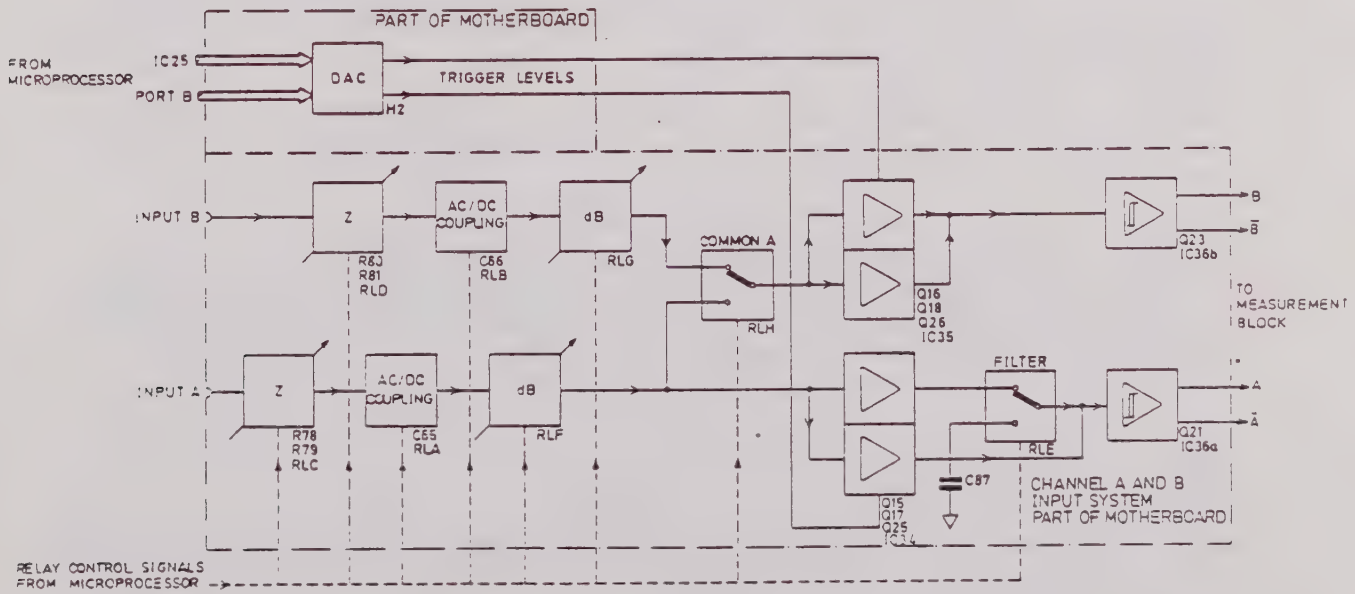


Figure 5.2 - Channel A/B Block Diagram

5.3.1.2 Circuit Description

5.3.1.2.1 Refer to the schematic shown on page 7-10. When relay RLC is energized, the input impedance seen at SK5 (INPUT A) is 50Ω , given by resistors R78 and R79 in parallel.

5.3.1.2.2 When energized, RLA gives DC coupling of the input signal. With RLA deenergized, the signal is AC coupled via C65. R165 limits the current surge which occurs if DC coupling is selected while C65 is in the charged state.

5.3.1.2.3 The x1/x10 attenuator is formed by R82, R83, R87 and RLF. With RLF deenergized, the attenuator has a series element, R82, and a shunt element formed by R83 and R87 in parallel. The attenuation is 20 dB (nominal). With RLF energized R82 is short-circuited, giving 0 dB attenuation.

5.3.1.2.4 The attenuator output is fed to the high-frequency channel buffer, Q15 and Q17, via R160 and C73. The gate of Q15 is protected against excessive negative voltage swings by D5. The gain from the attenuator output to the emitter of Q17 is approximately 0.94.

5.3.1.2.5 The buffer of the low frequency channel, IC34 and Q25, receives its input from the potential divider R87. The gain from R87 pin 1 to the emitter of Q25 is approximately 0.94. Any offset in the system can be nulled by adjusting R192.

5.3.1.2.6 When RLE is deenergized (Channel A filter not selected), the signals from the two buffers are combined at the base of Q21 by the network C79 and R107. These components act as a low-pass filter to the output of the low frequency buffer, and as a high-pass filter to the output of the high frequency buffer. The crossover frequency is 5 kHz.

5.3.1.2.7 The signal at Q21 emitter is fed to the Schmitt trigger IC36a via the diode bridge formed by D18, D19, D20, and D21. This protects the input of IC36a by limiting the signal swing to approximately ±1V.

5.3.1.2.8 The differential output of IC36 forms the input to the measuring block. The hysteresis of IC36, and therefore the channel sensitivity, can be set by adjusting R149.

5.3.1.2.9 The trigger level is set by the DAC, H2, shown on page 7-11 and is fed to IC34-2 via R202 and one section of R89. Feedback, taken from the emitter of Q21 to IC34-2 via R89 pins 5 and 3, makes R89 pin 3 a virtual ground point, and the gain from the R136/R202 junction to the emitter of Q21 is -0.94. A 1 VDC level at the Channel A input and a 1V trigger level, therefore, combine to give 0V at Q21's emitter. Thus, the selected trigger point on the input signal is always brought to 0V at Q21's emitter.

5.3.1.2.10 When Channel A's low-pass filter is selected, RLE is energized. This opens the high-frequency channel circuitry and connects C87 across the low frequency channel. The low-frequency channel bandwidth is then nominally 50 kHz.

5.3.1.2.11 The circuit of Channel B is similar to that of Channel A, but is not provided with a low-pass filter. Energizing RLH connects the signal applied at the Channel A input to both channel amplifiers.

5.3.1.2.12 The relays are controlled by the microprocessor. The voltage levels on the control lines are latched in IC24 as shown on page 7-11.

5.3.2 CHANNEL C BLOCK

5.3.2.1 Functional Description

5.3.2.1.1 Refer to the block diagram given in Figure 5.3. Channel C processes the signal applied at the Channel C input and feeds it to the measurement block.

5.3.2.1.2 Channel C's input is protected by a fuse, mounted in the input connector, and by a signal-limiting circuit. Next is an automatic level control circuit which reduces the range of the signal level applied to the amplifier.

5.3.2.1.3 After amplification, the signal is prescaled by 64 before being passed via a buffer and a signal gate to the measurement block.

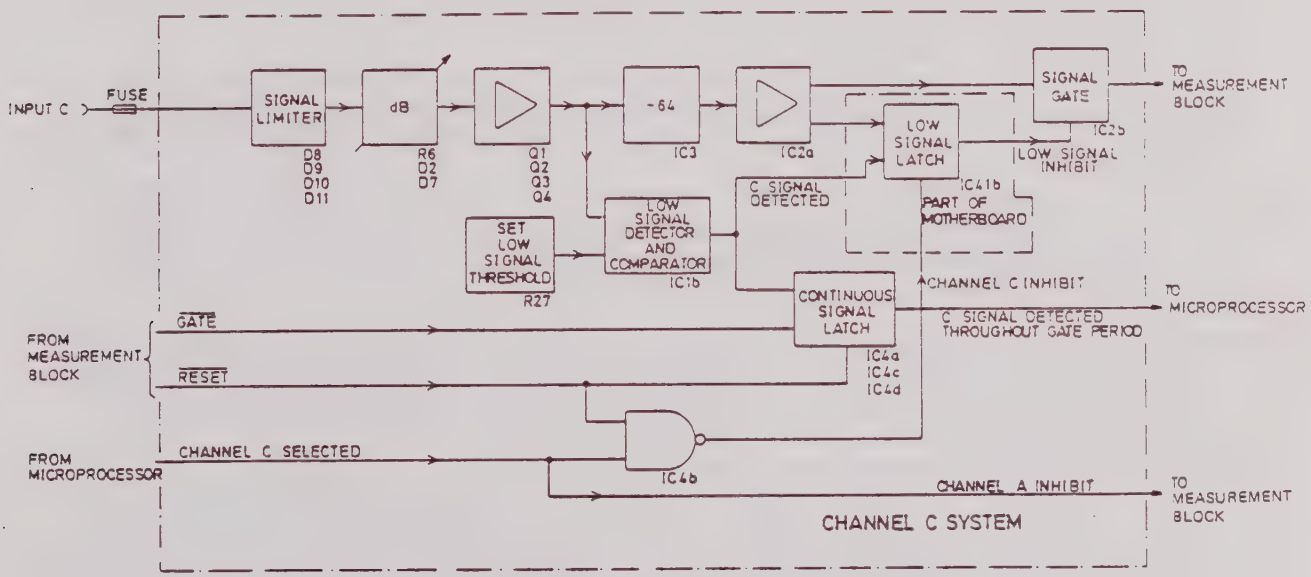


Figure 5.3 - Channel C Block Diagram

5.3.2.1.4 The amplitude of the signal at the amplifier output is monitored by a detector and comparator. The comparator output controls the low-signal latch. If the detector output is below the threshold, the latch is set and the channel output is inhibited by the signal gate. When the detector output goes above the threshold, the low-signal latch is armed and opens the signal gate on the next signal edge from the prescaler. This enables the instrument to make measurements on signal bursts.

5.3.2.1.5 The detector output is also applied to the continuous signal latch. This latch is reset at the beginning of each gate period and is set if the detector output falls below the threshold level. The microprocessor samples the latch output throughout the gate period. If the measured signal falls below the threshold level during this period, the measured result is set to zero.

5.3.2.1.6 If Channel C is not selected, the low-signal latch is held in reset by a control signal from the microprocessor and the output to the measurement block is inhibited. The same control signal is used to enable Channel A so that the two channels cannot be enabled at the same time.

5.3.2.2 Circuit Description

5.3.2.2.1 Refer to the schematic shown on page 7-34. The signal to be measured is connected via SK13 (INPUT C). The circuit is protected by a fuse which is mounted within SK13. The signal amplitude is limited by the diode clamp comprised of D8, D9, D10, and D11.

5.3.2.2.2 A degree of automatic gain control is achieved by means of an attenuator, formed by R6 and the impedance of the PIN diodes D2 and D7. The peak-to-peak detector D1, D3, R7, and C48 produces a negative voltage proportional to the signal amplitude. A direct current proportional to this voltage flows through the PIN diodes via L1. The impedance of the diodes decreases if the current increases so that changes in signal amplitude are offset by changes in attenuation.

5.3.2.2.3 The signal passes through four amplifier stages incorporating Q1, Q2, Q3, and Q4. The amplified signal is fed to the counter IC3 via the shaping circuit formed by R37, C46, and R36.

5.3.2.2.4 The signal frequency is prescaled by 64 in IC3 and buffered in IC2a. Provided that Channel C is selected and the amplitude of the signal is adequate, the output at IC2a-2 passes to the measurement block via the gate IC2b and SK7 pin 5.

5.3.2.2.5 The signal at the output of Q4 is fed to the low-signal detector D5 and C23. The comparator IC1b compares the detector output with a threshold voltage set by R27. The comparator output is at logic 1 if the detector output is below the threshold (Channel C's signal amplitude too low for accurate counting).

5.3.2.2.6 The logic level at the comparator output is inverted in IC1-A and is fed via SK7 pin 14 to the D input (pin 10) of the low-signal latch IC41b shown on page 7-11. IC41b is clocked by the output of IC2-A via SK7 pin 8. If the signal from Q4 is below the threshold, IC41b-14 goes to logic 1. This level is fed back via SK7 pin 7 to disable the gate IC2-B and inhibit the output to the measurement block.

5.3.2.2.7 The $\overline{\text{GATE}}$ signal enters the system at SK7 pin 17 and is inverted in IC1-C. The resulting signal and the output of the comparator IC1-B are fed to IC4-A. If both inputs are at a logic 1, indicating that the Channel C signal level is too low while the gate is open, the continuous signal latch IC4-C and IC4-D is set. The latch output is fed to the microprocessor via SK7 pin 11 and prevents the result of any measurement made during that gate period from being displayed.

5.3.2.2.8 The U signal at SK7 pin 16 is at a logic 1 when Channel C is selected. A buffered version of this signal is fed to SK7 pin 1 via IC2-C and disables Channel A at IC41a shown on page 7-11. When Channel C is not selected, SK7 pin 16 is at logic 0. This level is inverted and buffered in IC4-B and IC1-D, and is then fed to IC41b via SK7 pin 13. IC41b is held in reset, inhibiting the Channel C signal at IC2-B via SK7 pin 7.

5.3.3 Measurement Block

5.3.3.1 Functional Description

5.3.3.1.1 The measurement circuits of the instrument are provided by three custom-built integrated circuits. These are the two Multiple Counter and Control (MCC) circuits, MCC1 and MCC2, and the Timing Error Correction (TEC) circuit. A block diagram is shown in Figure 5.4.

5.3.3.1.2 The circuits within MCC1 and MCC2 are configured by the microprocessor according to the measurement function selected. The recipromatic counting technique is used. With this technique the measured signal, not the counter clock pulses, controls the start and stop of the measurement period (gate time) as shown in Figure 5.5. The gate time, therefore, extends over an integral number of cycles of the measured waveform. The gate time is measured by counting the clock pulses which occur while the gate is open. This leads to timing errors at both ends of the gate time, as shown. The TEC circuit enhances the measurement accuracy by compensating for these errors.

5.3.3.1.3 For all measurement functions except FREQ A and PERIOD A, the signals to be measured are fed directly to MCC2. For FREQ A and PERIOD A, the Channel A signal is scaled by two and fed to the $\overline{C}$ input of MCC2. When FREQ C is selected, the prescaler is disabled by the CHANNEL A INHIBIT signal from the Channel C block.

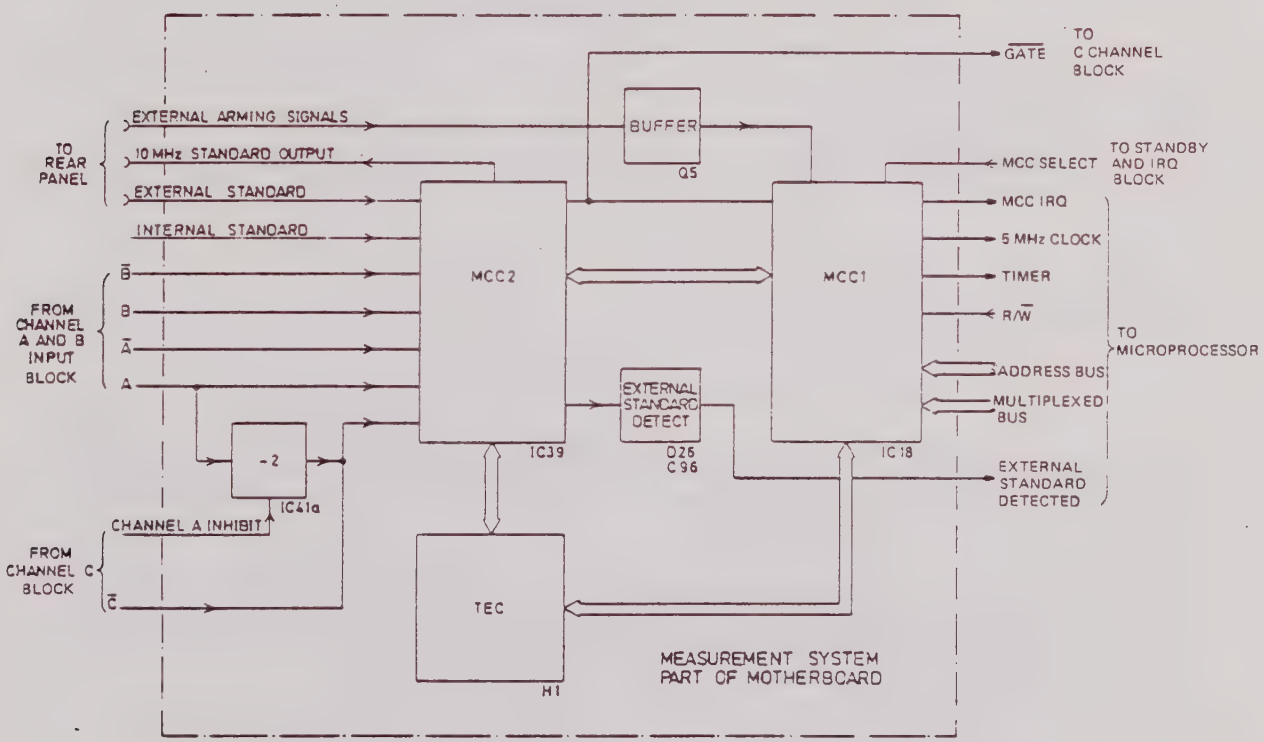


Figure 5.4 - Measurement - Block Diagram

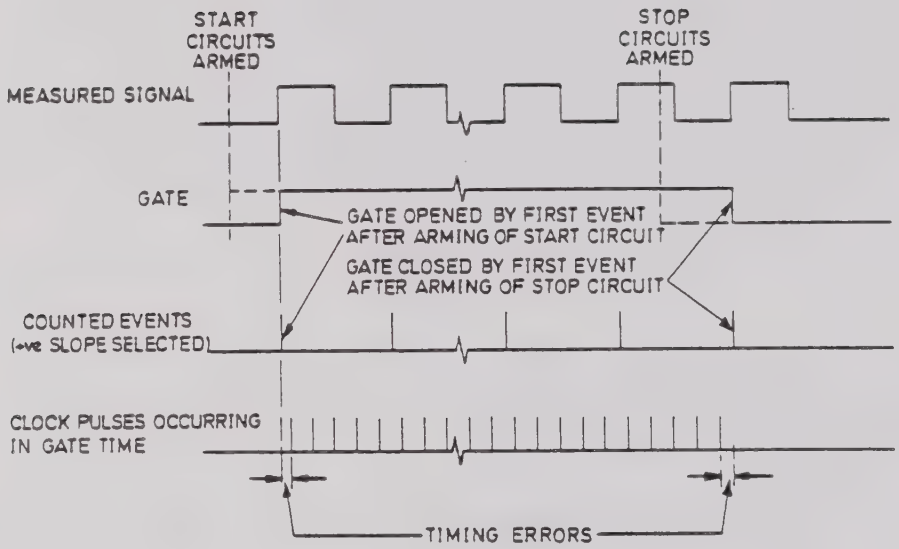


Figure 5.5 - Basic Reciprocatic Counting Technique

5.3.3.1.4 At the end of each measurement period, MCC1 generates an interrupt request for the microprocessor. The registers within MCC1 are addressed using the address bus and the MCC SELECT line. The measured value is transferred to the microprocessor via the multiplexed bus.

5.3.3.1.5 The internal and external frequency standard inputs are both fed to MCC2. The system will operate from the external standard provided that the input is of sufficient amplitude. A 10 MHz output, derived from the frequency standard in use, is made available at a socket on the rear panel.

5.3.3.2 Circuit Description

5.3.3.2.1 Refer the the schematic shown on page 7-11.

5.3.3.2.2 Measured Signal Input

5.3.3.2.2.1 For all measurement functions other than FREQ A and PERIOD A, the differential outputs from Channel A and Channel B are applied to the measuring circuit at IC39-15, 16, 17 and 18. For the FREQ A and PERIOD A functions, the A signal frequency is divided by two in IC41a and fed to IC39-19.

5.3.3.2.2.2 For the FREQ C and RATIO C/B functions, the $\overline{C}$ signal is fed to IC39-19. For these functions IC41a-5 is held at logic 1 by the PST1 control line (CHANNEL A INHIBIT) from the Channel C block. As a result, IC41a is held in set and the A signal is inhibited from reaching IC39-19.

5.3.3.2.3 Reference Frequency

5.3.3.2.3.1 The internal reference signal is applied to IC39-2 and the external reference signal, if present, to IC39-3. A buffered version of the external reference is present at IC39-24 and is applied to the detector D26, C96, and R129. The detector output is fed to IC23-6 and is read periodically by the microprocessor. If the level is above the TTL logic 1 threshold, the microprocessor sets IC39-38 to logic 0 and the measurement block switches to use the external reference.

5.3.3.2.3.2 A 10 MHz signal, derived from the frequency standard, is present at IC39-37 and is fed to the 10 MHz STD OUTPUT socket on the rear panel via PL19 pin 2.

5.3.3.2.3.3 A 10 MHz reference signal, derived from the frequency standard, is present at IC39-36. This signal is applied to the TEC, H1, at pin 6, and, after inversion in IC29e, to IC18-24.

5.3.3.2.4 Microprocessor Clock and Timer

5.3.3.2.4.1 A 5 MHz clock signal for the microprocessor (and the GPIB microprocessor if fitted) is taken from IC18-2. A 39.0625 kHz clock signal for the microprocessor timer is taken from IC18-4.

5.3.3.2.5 Channel C Gate and Reset

5.3.3.2.5.1 A $\overline{\text{GATE}}$ signal (logic 0 during the measurement period) and a $\overline{\text{RESET}}$ signal (negative-going pulse at the end of each measurement period) are taken from IC39-27 and IC18-40 and fed to the Channel C block via PL7 pins 17 and 15.

5.3.3.2.6 External Arming Input

5.3.3.2.6.1 Signal connected to the EXT ARM INPUT socket on the rear panel are fed to IC18-27 via PL19 pin 1 and the amplifier stage Q5.

5.3.3.2.7 Control Signals

5.3.3.2.7.1 The logic levels on lines Q0 to Q4, between IC18 and IC39 are shown in Table 5.1. These levels are stable if the following conditions exist:

a. No signals are applied to any of the channel inputs

b. Auto-trigger is disabled on Channels A and B

Table 5.1 - Control Logic Levels by Function

Measurement	Control Line				
Function:	Q0	Q1	Q2	Q3	Q4
FREQ A	1	1	0	1	0
PERIOD A	1	1	0	1	0
FREQ B	1	0	0	1	0
PERIOD B	1	0	0	1	0
FREQ C	1	1	0	1	0
T.I. A→B	0	0	1	1	0
T.I. B→A	0	0	0	1	0
TOTAL A by B	1	0	0	1	1
TOTAL B by A	1	0	1	1	1
RATIO C/B	1	1	0	1	1
RATIO A/B	1	0	1	1	1
Special Function 72	1	1	1	0	1
Special Function 73	1	1	1	0	0
Special Function 74	1	1	1	0	1
Special Function 75	1	1	1	0	0

NOTES:

a. The FREQ B, PERIOD B, TOTAL B by A, and T.I. B→A functions are obtained using Special Function 21.

b. Special Functions 72 to 75 can only be used when CHECK is selected.

5.3.4 Display Block

5.3.4.1 Functional Description

5.3.4.1.1 A simplified diagram of the display block is given in Figure 5.6. The GPIB LEDs, GATE LED, Channels A and B TRIGGER LEDs, and the STANDBY LED are held on or off by control signals from other systems. The remainder of the display is multiplexed under the control of the display drivers.

5.3.4.1.2 To update the display, the microprocessor selects the appropriate display driver using the MODE 1 and MODE 2 control lines. A string of nine 8-bit words (a control word and eight data words) is then put onto the bus. Each word is entered into a memory within the display driver under the control of the STROBE signal.

5.3.4.1.3 The display driver then sequentially puts the data words onto its output bus. For each data word, the appropriate numeric indicator or group of LEDs is enabled by a signal on its control line.

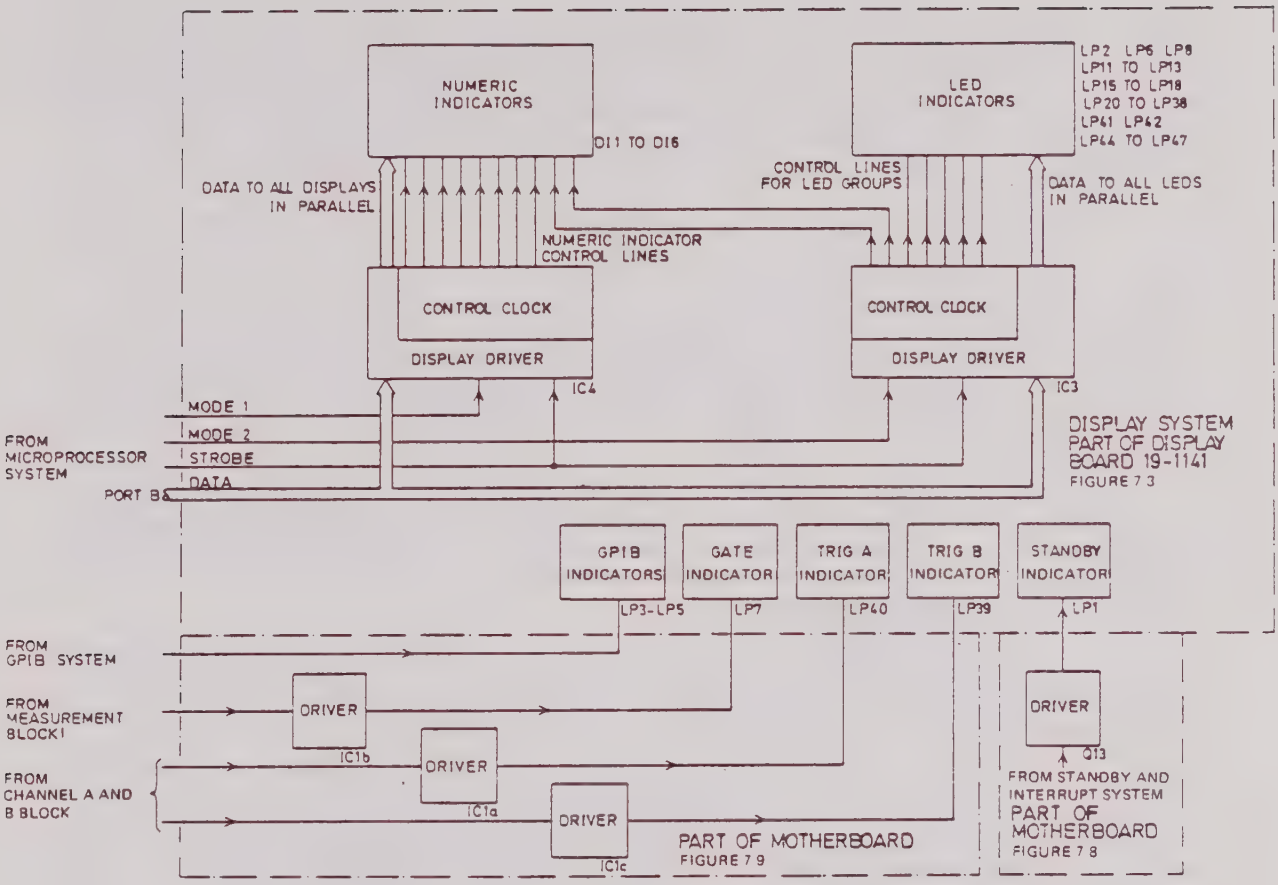


Figure 5.6 - Display-Block Diagram

5.3.4.2 Circuit Description

5.3.4.2.1 The schematic is shown on page 7-15. The GPIB LEDs LP3, LP4, and LP5 are driven via SK1 from the GPIB system. The GATE LED LP7 is driven from the measurement block via a driver stage, shown on page 7-12, and SK2 pin 11. The TRIG LEDs LP39 and LP40 are driven from the Channel A/B block via driver stages, shown on page 7-12, and SK2 pins 7 and 3. The STANDBY LED LP1 is driven via SK1 pin 8 from the standby and interrupt block. The remaining LED indicators and the numeric indicators DI5 and DI6 are controlled by the display driver IC3. Numeric indicators DI1 to DI4 are controlled by IC4.

5.3.4.2.2 Display data is stored in memory within IC3 and IC4. To change the data, the microprocessor puts a control word on the port B bus. The microprocessor writes this word into the display driver by means of a negative pulse applied to the DISPLAY STROBE line at SK1 pin 4. The control word determines the operating mode of the display drivers.

5.3.4.2.3 The microprocessor then selects the display driver required by setting a logic 0 on the appropriate MODE line at SK1 pin 3 or 6. Eight words containing display data are written into the selected display driver via the port B bus, controlled by eight negative-going pulses on the DISPLAY STROBE line.

5.3.4.2.4 The output of each display driver is multiplexed under the control of an internal clock. Eight-bit display data (for seven segments + decimal point or eight LED indicators) are put onto the device output bus (pins 1 to 4 and 24 to 27). A positive pulse is then applied to the enablement line of the device or group of indicators which is to display the data. The enablement line waveforms consist of 500 μs positive-going pulses at approximately 250 pps.

5.3.5 Keyboard Block

5.3.5.1 Functional Description

5.3.5.1.1 A simplified diagram of the keyboard block is given in Figure 5.7. The encoding of the keyboard data is performed within the system without microprocessor action. An interrupt request (IRQ) is made to the microprocessor when encoding is complete. Data transfer is initiated by the KEYBOARD ENABLE signal from the microprocessor.

5.3.5.1.2 The 32 keys are divided into two 16-key matrices. When a key is pressed, its position is encoded into a 5-bit word. One bit, carried on the $\overline{\text{KEYBOARD EXTEND}}$ line, indicates the matrix in which the key is located. The remaining bits indicate the position of the key within the matrix.

5.3.5.1.3 When a key is pressed, the encoder examines both matrices simultaneously and generates a 4-bit code representing the key position. The same four bits are generated regardless of the matrix in which the key is located.

5.3.5.1.4 If the key pressed is in the extended key matrix, one of the inputs to the NAND gate is pulled low. The $\overline{\text{KEYBOARD EXTEND}}$ line is then set to logic 0. If the key is in the non-extended matrix, the inputs to the NAND gate are isolated from the key line by one of the diodes and the $\overline{\text{KEYBOARD EXTEND}}$ line remains at logic 1.

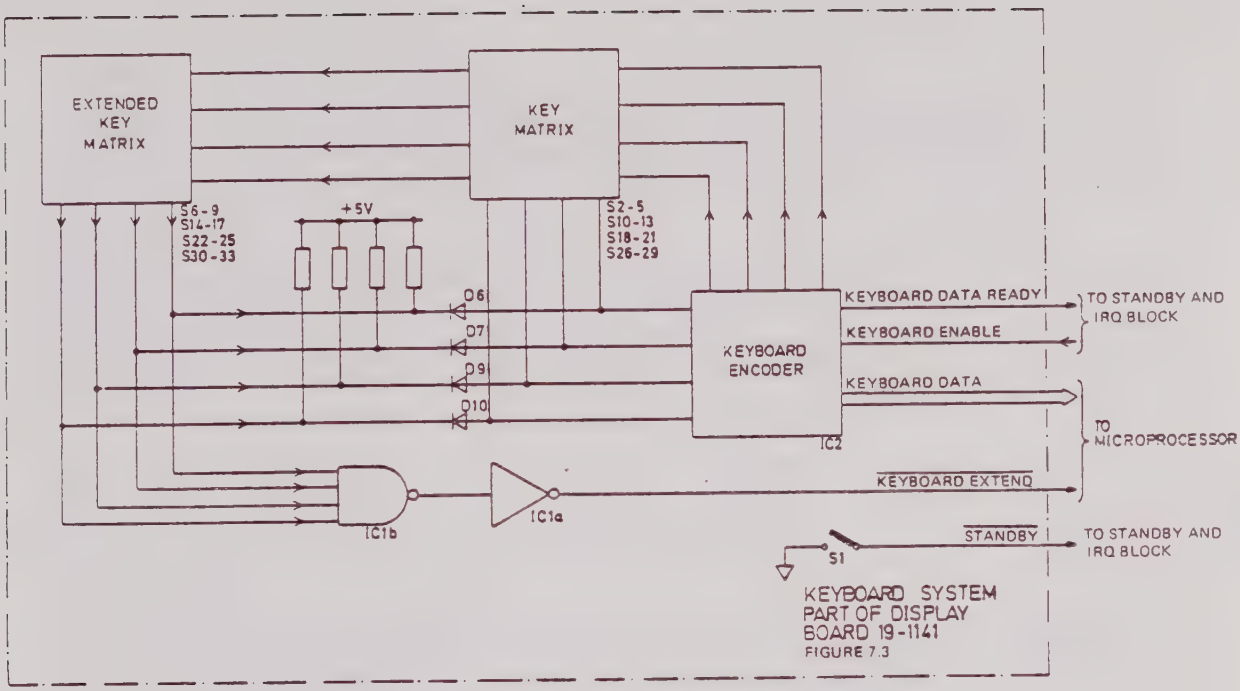


Figure 5.7 - Keyboard-Block Diagram

5.3.5.2 Circuit Description

5.3.5.2.1 The schematic is given on page 7-15. The keys are divided into two 16-key matrices having common row lines connected to the encoder at IC2-7, 8, 10, and 11. The matrices have separate column lines connected in pairs to IC2-1, 2, 3, and 4.

5.3.5.2.2 The encoder normally holds the row lines at logic 0. When a key is pressed, the corresponding column line is pulled to logic 0. The encoder then scans the keyboard and stores a 4-bit code, corresponding to the row and column of the key, in an internal register. Because the column lines are connected to the encoder in pairs, it cannot find which matrix contains the key.

5.3.5.2.3 The $\overline{\text{KEYBOARD EXTEND}}$ line indicates which matrix contains the key that is pressed. The inputs to IC2 are normally held at logic 1 so that SK2 pin 9 is at logic 1. If a key in the extended matrix (column lines connected directly to the inputs of IC1b) is pressed, one input of IC1b is pulled to logic 0 and SK2 pin 9 will go to logic 0. The column lines of the other matrix are isolated from the inputs of IC2 by D6, D7, D9, and D10, so that the logic level at SK2 pin 9 is not changed when a key in this matrix is pressed.

5.3.5.2.4 When the key-position code has been stored, the encoder sets the KEYBOARD DATA READY line, at SK2 pin 4, to logic 1 giving a microprocessor interrupt. The microprocessor sets IC2-13 to logic 0 using the $\overline{\text{KEYBOARD ENABLE}}$ line, and the encoder puts the 4-bit code onto the bus. The microprocessor reads the code and the state of the $\overline{\text{KEYBOARD EXTEND}}$ line to determine which key has been pressed.

5.3.6 Microprocessor Block

5.3.6.1 Functional Description

5.3.6.1.1 A simplified diagram of the microprocessor block is given in Figure 5.8. The microprocessor used has a 5-bit bus for the high-order address bits and an 8-bit multiplexed bus which is used for the low-order address bits and for data. The low-order address bits are strobed into the address latch, which holds them on an 8-bit address bus, to free the multiplexed bus for data.

5.3.6.1.2 Two latches, fed from port B of the microprocessor, are used to maintain voltage levels on the instrument control lines. A third latch is used to read the status of the instrument flags via port B. The latches and registers for the connection of the multiplexed bus to the measurement system are in the measurement block, and are controlled by the MCC SELECT signal. The display data latches are in the display block, and are controlled by strobe and chip select signals obtained from port A.

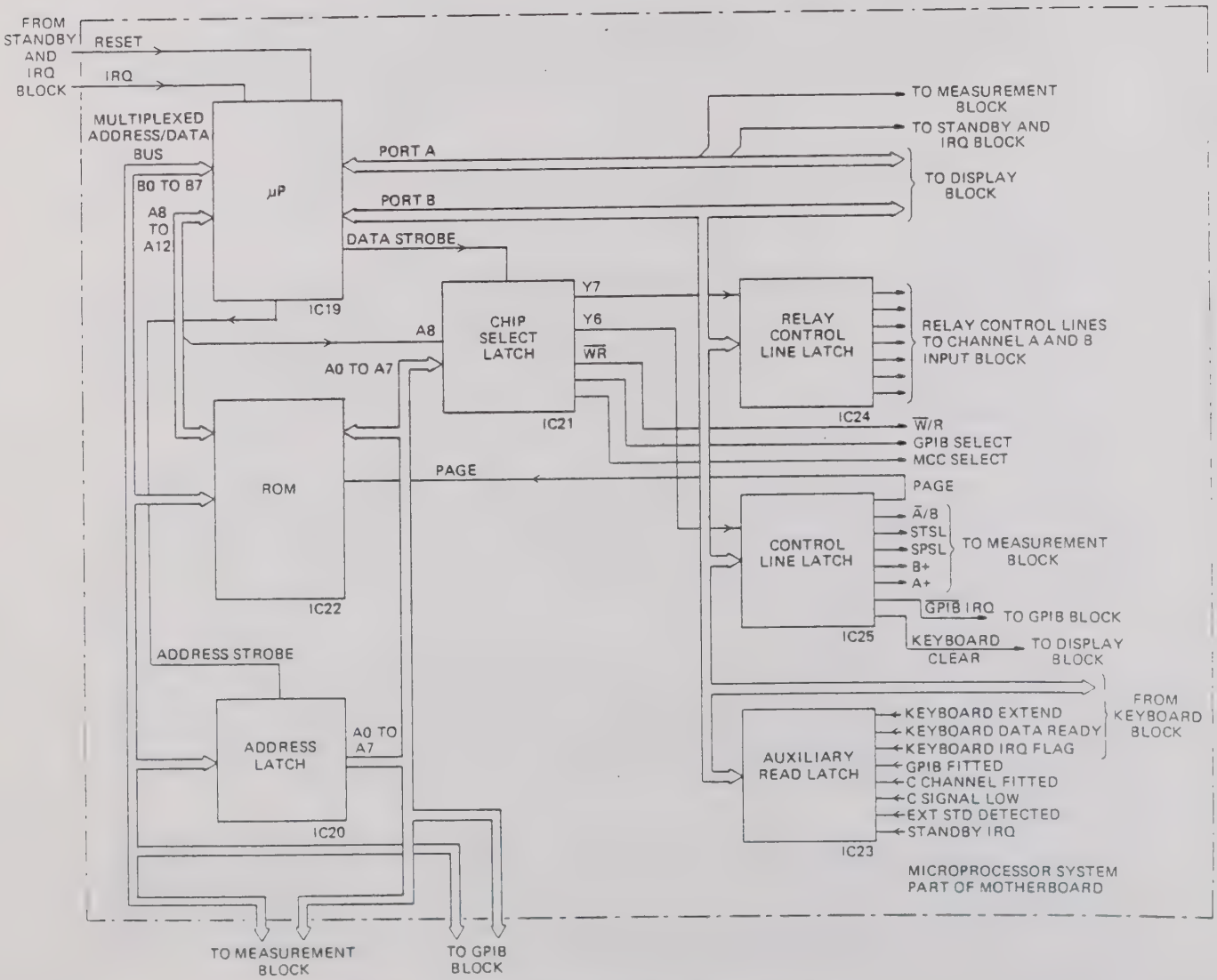


Figure 5.8 - Microprocessor-Block Diagram

5.3.6.2 Circuit Description

5.3.6.2.1 The schematic is given on page 7-11. The microprocessor clock and timer signals are generated in the measurement block and are fed to IC19-39 and IC19-37. A RESET signal is generated in the standby and IRQ block when the instrument is switched on or off and is fed to IC19-1.

5.3.6.2.2 The microprocessor bus for the high-order address bits is designated A8 to A12. The multiplexed bus, used for the low-order address bits and for data is designated B0 to B7. The microprocessor also has two input/output ports PA0 to PA7 and PB0 to PB7.

5.3.6.2.3 Multiplexed Bus Operation

5.3.6.2.3.1 The microprocessor puts IC19-6 (ADDRESS STROBE) at logic 1 and (DATA STROBE) at logic 0. This enables the address latch IC20 (IC20-11 at logic 1), disables ROM IC22 (IC22-20 at logic 1), and disables the address decoder IC21 (IC21-6) at logic 0).

5.3.6.2.3.2 This address is put onto lines B0 to B7 and A8 to A12. When the lines have settled, the ADDRESS STROBE line is taken to logic 0. The low-order bits of the address are latched into IC20 and are held on address lines A0 to A7. Lines B0 to B7 are now free for use as a data bus.

5.3.6.2.4 Address Decoding

5.3.6.2.4.1 The levels on address lines A6 to A12 are decoded in IC21 to provide the following outputs:

a. $\overline{\text{MCC SEL}}$, the chip-select signal for IC18

b. $\overline{\text{GPIB SEL}}$, the chip-select for the GPIB address decoder

c. $\overline{\text{WR}}$, the write control signal for H2

d. Y6, the chip select signal for output latch IC25

e. Y7, the chip select signal for output latch IC24

5.3.6.2.4.2 These outputs are only available when IC21 is enabled by a logic 1 at IC21-6 and a logic 0 at IC21-4,5. The level at IC21-6 is set by the DATA STROBE output at IC19-4, which is at logic 1 when the multiplexed bus is available for data transfer. All outputs from IC21 are decoded from addresses with lines A9 to A12 at logic 0 when IC21-4, 5 are held at logic 0 by the output from IC27a, b, and d.

5.3.6.2.5 Input and Output Latches

5.3.6.2.5.1 The logic levels required on the instrument control lines and on the PAGE line (most significant bit of RAM address) are set into the output latches IC24 and IC25 from data port B of the microprocessor. The latch strobe signals are decoded in IC21. Data may be read by the microprocessor from the input latch IC23. The latch strobe signal is provided via data port A of the microprocessor.

5.3.7 Standby and IRQ Block

5.3.7.1 Functional Description

5.3.7.1.1 This block generates reset signals for the microprocessor and GPIB interface, and the standby switching signal for the power supply system. It also combines the IRQ signals from the GPIB interface, the measurement block, and the keyboard block for connection to the microprocessor. A block diagram is given in Figure 5.9.

5.3.7.1.2 Reset signals for the microprocessor and the GPIB interface are generated whenever power is applied to or removed from the instrument's power supply system.

5.3.7.1.3 On switching to standby, the standby signal from the keyboard block sets the standby IRQ latch. The latch outputs provide the standby IRQ and a standby flag for the microprocessor. The standby IRQ output also clocks the standby ON/OFF latch to the set state. This provides signals to switch the power supply to standby, light the STANDBY LED, and disable IC30b, thereby inhibiting the other IRQs. At the end of the microprocessor interrupt routine, the standby IRQ latch is reset, removing the standby IRQ. The state of the standby ON/OFF latch is not changed.

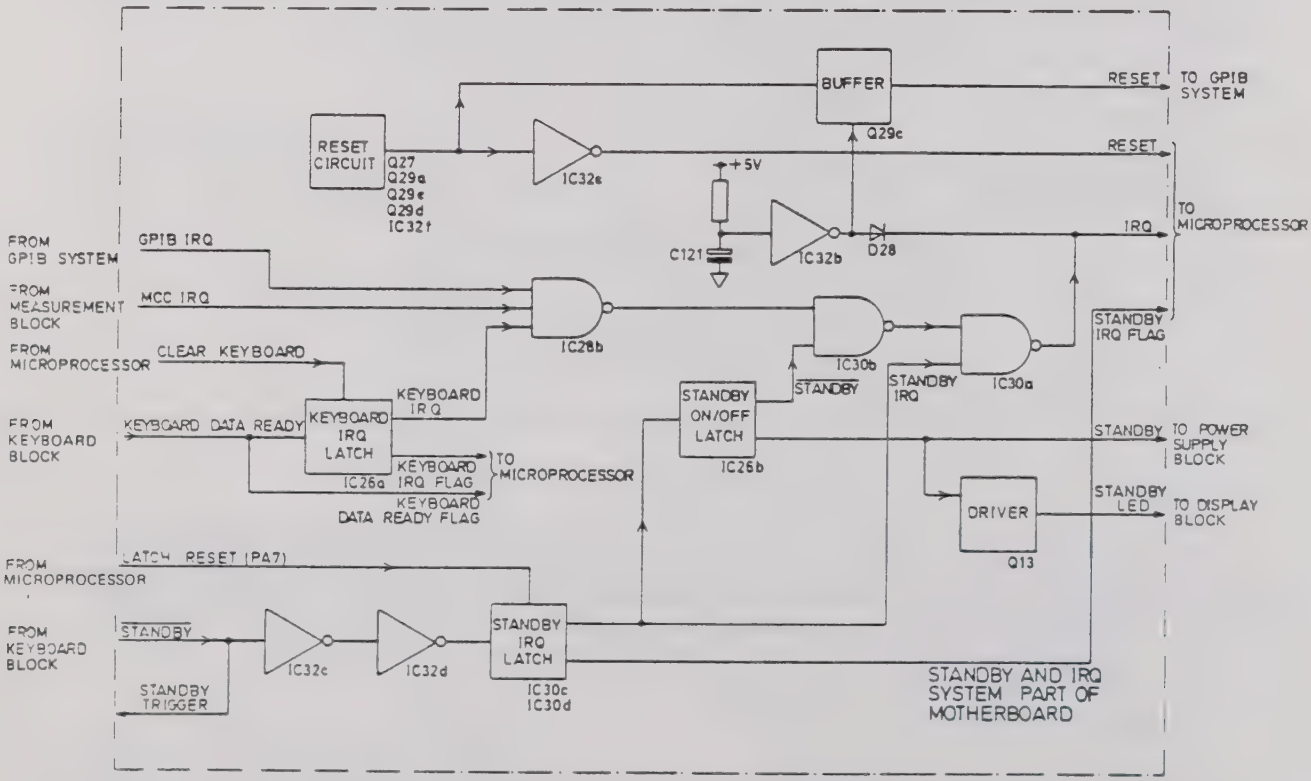


Figure 5.9 - Standby and IRQ Block Diagram

5.3.7.1.4 While the instrument is in standby, the input to IC32b is held low and the IRQ input to the microprocessor is held high via D28. This inhibits all IRQs. The output from IC32b also holds the GPIB interface in reset via Q29c.

5.3.7.1.5 On return from standby, the standby IRQ latch is again set by the standby signal from the keyboard block. The standby ON/OFF latch is clocked to the reset state, the power supply is returned to normal operation, and IC30b is enabled. The input to IC32b rises as C121 charges, removing the reset signal from the GPIB interface and enabling the microprocessor IRQ input. The microprocessor is now able to accept the IRQ from IC30a. At the end of the restart sequence, the standby IRQ latch is reset.

5.3.7.1.6 When the encoder in the keyboard system has data ready to be read by the microprocessor, the keyboard IRQ latch is clocked via the KEYBOARD DATA READY line. The latch outputs provide the keyboard IRQ and a keyboard IRQ flag. Once the keyboard has been identified as the source of the interrupt, the latch is reset by the microprocessor.

5.3.7.2 Circuit Description

5.3.7.2.1 The schematic is shown on page 7-11.

5.3.7.2.2 Reset Circuit

5.3.7.2.2.1 The $\overline{\text{RESET}}$ signal is generated in the circuit containing Q27, Q29a, d, and e, and C125. When the instrument is switched on, the input to IC32f is held low until C125 charges through R215, Q29a, and R216. The output at IC32f-12 goes to logic 1 when power is applied, but drops to logic 0 after approximately 500 ms. This output is inverted by IC32e to provide the microprocessor reset and by Q29c to provide the GPIB reset.

5.3.7.2.2.2 If there is a reduction in the +5V STANDBY supply, due to the instrument being switched off or to power failure, the potential across R217 falls. The potential at Q27 emitter is maintained by the charge in C125, so Q27 conducts. The current in R218 makes the base of Q29d positive, so the transistor conducts and holds the base of Q27 low until C125 is completely discharged. This ensures that a good reset action is obtained, even if the power is quickly restored.

5.3.7.2.3 Standby Operation

5.3.7.2.3.1 On switching to standby, PL1 pin 14 is taken to 0V by the STANDBY key. Debouncing is provided by R158 and C126. The leading edge of the signal is sharpened in IC32c, C118, R151, and IC32d, and sets the standby IRQ latch IC30c, d.

5.3.7.2.3.2 The negative-going output from IC30c-10 is passed via IC30a, IC32a, and R152 to IC19-2 to provide a microprocessor interrupt. The positive-going output from IC30d-11 forms the standby IRQ flag (read by the microprocessor via IC23 during the interrupt routine) and clocks the standby latch IC26b to the set state.

5.3.7.2.3.3 The logic 0 level at IC26b-8 switches on Q13 and provides power for the STANDBY LED via PL1 pin 8. The same output is applied to IC30b-5 and disables the other interrupts which are connected to IC30b-6.

5.3.7.2.3.4 The logic 1 level at IC26b-9 shuts down the power supplies except the +5V STANDBY supply.

5.3.7.2.3.5 At the end of the interrupt routine, the microprocessor resets the standby IRQ latch by applying logic 1 to IC30c-8 from IC19-7.

5.3.7.2.3.6 On return from standby, the standby IRQ latch is again set. This provides a microprocessor interrupt and sets the standby IRQ flag as before. The positive-going output from IC30d-11 clocks the standby latch back to the reset state, so that the STANDBY LED is turned off and the power supplies are restored. The microprocessor resets the standby IRQ latch at the end of the interrupt routine.

5.3.7.2.4 The IRQ Circuits

5.3.7.2.4.1 The KEYBOARD DATA READY line at PL2 pin 4 goes to logic 1 when the keyboard encoder has data available. This clocks IC26a to the set state to provide a keyboard IRQ flag at IC23-11 and an interrupt signal at IC28b-9. Interrupts from the measurement system ($\overline{\text{MCC IRQ}}$) and the GPIB interface ($\overline{\text{GPIBIRQ}}$) are connected to IC28b-12 and IC28b-10, 13.

5.3.7.2.4.2 If any of these interrupts occur, IC28b-8 and IC30b-6 will go to logic 1. Provided the standby latch IC26b is not set, IC30b-5 will be at logic 1 and the interrupt signal passes via IC30a and IC32a to IC19-2.

5.3.7.2.4.3 When the instrument is switched into or out of the standby state, the standby IRQ latch IC30c, d is set. The standby IRQ from IC30c-10 is fed to IC19-2 via IC30a and IC32a.

5.3.7.2.4.4 The circuit comprising R220, C121, IC32b, and D28 disables the microprocessor interrupt input and holds the GPIB microprocessor reset line low (via Q29c), while the +5V power supply to R220 is switched off. On return from standby, C121 charges and IC32b-4 goes to logic 0. The microprocessor interrupt input is enabled and the GPIB microprocessor is reset. The delay in enabling the interrupts prevents the standby IRQ, which occurs on return from standby, from being acted upon before the power supplies are fully restored.

5.3.8 Power Supply Block

5.3.8.1 Functional Description

5.3.8.1.1 A simplified diagram of the power supply block is given in Figure 5.10. The AC supply enters at a plug mounted on the rear panel and passes via a fuse and RFI filter, mounted on the motherboard, to the line switch.

5.3.8.1.2 The switched supply is connected to the primary winding of the power transformer via the operating-voltage range selector. The voltage range selector is a small plug-in printed circuit board which is positioned according to the desired line voltage.

5.3.8.1.3 The transformer has a tapped secondary winding which supplies two bridge rectifiers. The smoothed but unregulated outputs from the rectifiers feed regulators providing +11.2V, -11.2V, +5V, +5V and -5.2V. The -5.2V regulator and one of the +5V regulators, which supply most of the instrument's circuits, are shut down by a signal from the microprocessor when the instrument is switched to standby.

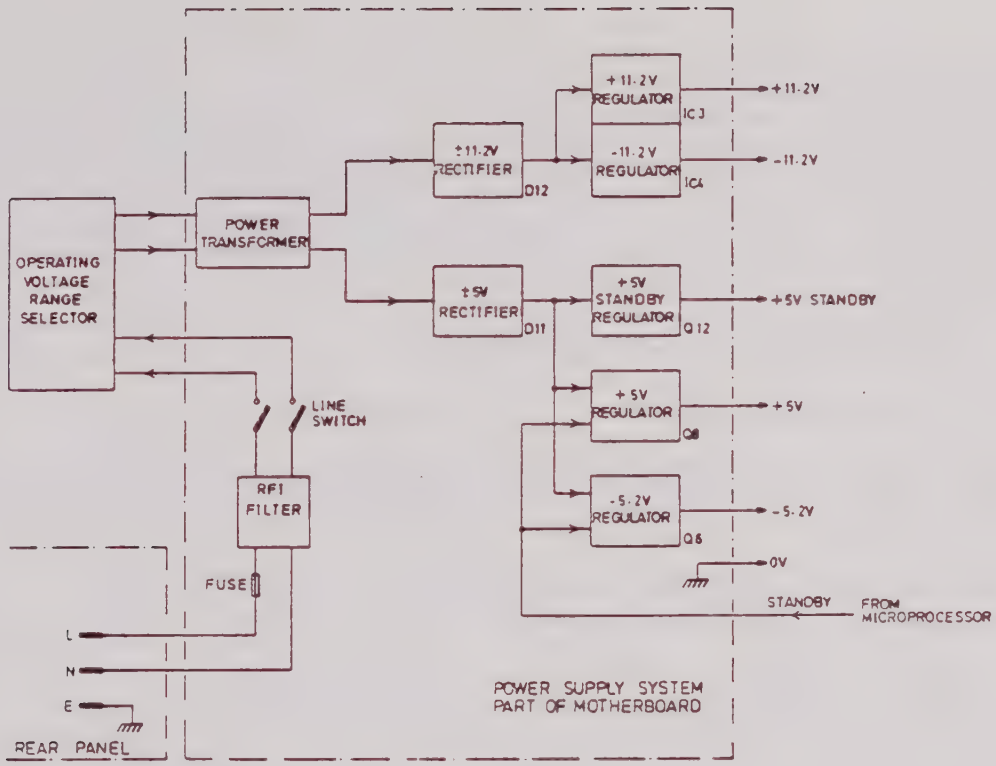


Figure 5.10 - Power-Supply-Block Diagram

5.3.8.2 Circuit Description

5.3.8.2.1 The schematic is shown on page 7-12. AC power connected at the power input plug passes via fuse FS1 and the RF filter, formed by L1, L2, C46, C47, and C48, to the POWER switch S1b. The switched supply is connected to the primary windings of transformer T1 via the tracks of a printed circuit board which is inserted in SK8.

5.3.8.2.2 The secondary windings fo transformer T1 suppy the ±5V rectifier D11, C49 and C50, and the ±11V rectifier D12, C52, and C59.

5.3.8.2.3 Regulated supplies at ±11.2V are provided by the regulators IC3 and IC4. The common terminals of these regulators are held at approximately -0.7V and +0.7V by diodes D13 and D14.

5.3.8.2.4 Regulated supplies at +5V are provided by two discrete component regulators having series elements Q8 and Q12. The non-inverting inputs to the comparators IC31a and IC31c are connected to a +2.5V reference voltage, derived in the hybrid circuit H2 shown on page 7-11. Potential dividers formed by elements of R49 hold each inverting input at half the output voltage of the associated regulator.

5.3.8.2.5 A regulated supply at -5.2V is provided by a discrete component regulator having Q6 as its series element. The comparator inputs are held at approximately 0V. The potential divider controlling the inverting input is connected across the +5V and -5.2V supplies.

5.3.8.2.6 Standby Mode

5.3.8.2.6.1 When the instrument is switched to standby, the standby latch IC26b (see page 7-11) is clocked to the set state. The base of Q11 is pulled high and IC31a-3 is pulled low. The base of Q9 is pulled low by IC31a, the base current of Q8 is cut off, and the regulator is shut down. When the voltage of the +5V supply falls, IC31b-6 goes more negative. The base of Q7 is taken towards 0V by IC31b so that the base current of Q6 is cut off and the -5.2V regulator is shut down.

5.3.9 Internal Frequency Standard Block

5.3.9.1 Functional Description

5.3.9.1.1 The internal frequency standard consists of a 5 MHz oscillator and a frequency doubler. A block diagram of the internal frequency standard is shown in Figure 5.11.

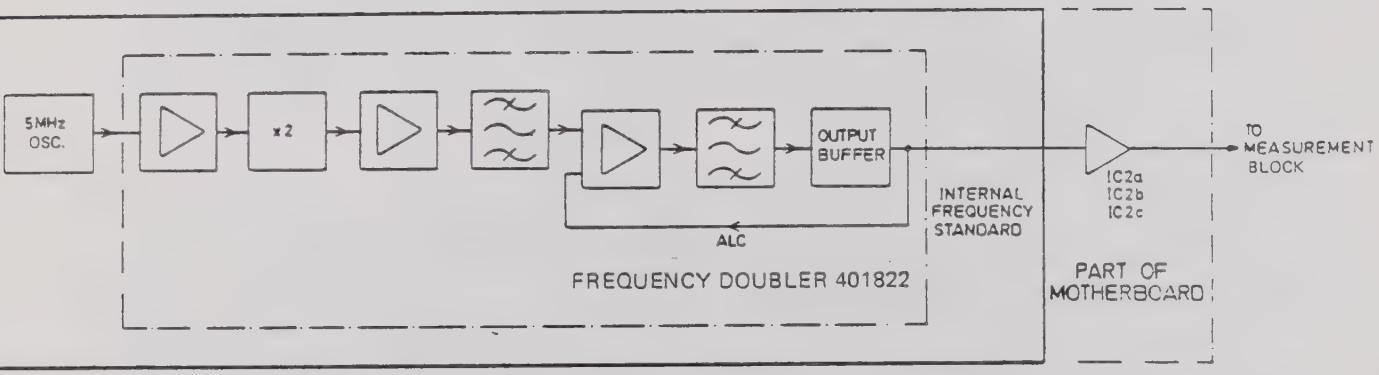


Figure 5.11 - Internal Frequency Standard Block Diagram

5.3.9.1.2 The 10 MHz signal is passed to the measurement block via a buffer (IC2) on the motherboard.

5.3.9.1.3 Signals from an external frequency standard are applied to a signal conditioning circuit on the motherboard. If a 10 MHz external frequency standard is used, the output of this circuit is connected directly to the measurement circuitry.

5.3.9.2 Circuit Description

5.3.9.2.1 Frequency Doubler

5.3.9.2.1.1 The schematic of the frequency doubler, used with the internal frequency standard is given on page 7-30. The 5 MHz input is applied to the balanced amplifier containing Q1 and Q2. The base of Q3 is driven by the differential outputs from the amplifier via D1 and D2 so that the frequency here is 10 MHz.

5.3.9.2.1.2 The 10 MHz signal is amplified and filtered in the two stages containing Q3 and Q5, and fed to pin 3 via buffer Q6.

5.3.9.2.1.3 The output signal is fed back via C6 to switch Q4 on during the positive peaks of the signal. The gain of Q5 is controlled by the potential across C3 which charges via R12 and discharges via Q4. If the output signal increases, the time for which Q4 conducts increases so that the mean potential across C3 decreases. The resulting decrease in gain of Q5 provides automatic level control.

5.3.9.2.2 Internal Frequency Standard Buffer

5.3.9.2.2.1 The buffer circuit is shown on page 7-12. The 10 MHz input at PL14 pin 4 is shaped and buffered in IC2a, IC2b, and IC2c before being fed to the measurement block at IC39-2. The inverting inputs of IC2 are connected to the bias voltage at IC2-11.

5.3.9.2.3 External Frequency Standard Buffer

5.3.9.2.3.1 The buffer circuit is shown on page 7-12. The signal connected to the EXT. STD. INPUT socket on the rear panel is fed to PL20 pin 4. Protection against excessive signal amplitude is provided by D6, D7, and R32.

5.3.9.2.3.2 The buffer comprises IC14a, IC14b, and IC14c. The inverting inputs are connected to the bias voltage at IC14-11. The final stage has feedback connected via R11 to give a Schmitt trigger action.

5.3.9.2.3.3 Link LK1 is fitted between pins 8 and 9 of the PL16 to connect the differential output of the final stage to the measurement block at IC39-3.

5.3.10 GPIB Interface

5.3.10.1 Introduction

5.3.10.1.1 The GPIB interface is a self-contained, microprocessor-controlled system. It handles the transfer of data between its internal memory and the GPIB without involving the main instrument's microprocessor. Data transfer is made one byte at a time, each transfer being controlled by the IEEE-488 handshake protocol. Refer to the schematic on page 7-18.

5.3.10.1.2 The microprocessor $\overline{\text{RESET}}$ signal is derived from the standby and IRQ block. The clock signal is derived from MCC1, IC18, shown on page 7-11.

5.3.10.1.3 The microprocessor uses a multiplexed bus, the eight low-order bits being used for both address and data. The low-order address bits are put onto the bus first and are latched into IC11 by the address strobe. The bus is then free for data use.

5.3.10.1.4 Data transfer between the microprocessors is initiated by an interrupt and is controlled by a 3-wire handshake protocol. The transfer is in the form of a data string, the number of bytes in the string being indicated by the first byte.

5.3.10.2 Address Setting and Recognition

5.3.10.2.1 The microprocessor reads the settings of the address switches in switchbank S1, via its port B inputs, approximately every 1 ms and writes the settings into an address register within the general purpose interface adapter (GPIA) IC12.

5.3.10.2.2 When the interface address is set on the bus by the controller, it is recognized by the GPIA by comparison with the contents of the internal address register.

5.3.10.3 Reading from the Bus

5.3.10.3.1 When the interface is addressed to listen, the GPIA conducts the handshake procedure up to the point where the ready for data (RFD) indication is given. At this point IC12-27 is at logic 0, giving a logic 1 level at IC18-11. This puts three of the bilateral switches of IC13 into the conducting state, thus completing the RFD line. The logic 0 at IC12-27 also puts the buffers in IC14 and IC15 into the receive condition. Data from the bus enters the GPIA data-in register and IC12-40 goes to logic 0 providing an interrupt request to the microprocessor IC9.

5.3.10.3.2 The microprocessor interrupt routine establishes the reason for the interrupt. The address decoder IC8 is enabled via IC27-15, IC26-8, and A7. The decoder is addressed using lines GA4, 5, and 6, and gives the GPIA enable signal at IC8-15. The data-in register of the GPIA is addressed using the R/W line and lines A0, 1, and 2. The microprocessor then reads the contents of the data-in register and transfers the data to memory.

5.3.10.3.3 When the data-in register has been read, the GPIA cancels the interrupt request and allows the data accepted (DAC) line to go high. The handshake routine then continues, and a further byte, if available is loaded into the data-in register. The interrupt and data transfer sequence is then repeated.

5.3.10.4 Writing to the Bus

5.3.10.4.1 When the GPIA is addressed to talk, its internal data-out register will normally be empty. Under these conditions IC12-40 goes to logic 0 and provides an interrupt request to the microprocessor.

5.3.10.4.2 IC17B is in the reset state, giving a logic 1 at IC18-12. Since IC12-27 is at logic 1 when the GPIA is addressed to talk, IC18-13 is also at logic 1. The resulting logic 0 at IC18-11 opens three circuits of bilateral switches in IC13 to break the RFD line. The fourth bilateral switch conducts, due to the logic 1 at IC19-10, and holds IC12-18 at 0V. Even if the listening device asserts that it is ready for data, IC12 will not attempt to load the contents of the data-out register onto the bus.

5.3.10.4.3 The microprocessor interrupt routine establishes the reason for the interrupt. The microprocessor then enables the address decoder, IC8, via IC27-15, IC26-8, and A7. The decoder is addressed using lines GA4, 5, and 6, and gives the GPIA enable signal at IC8-15. The data-out register of the GPIA is addressed using the R/W line and lines GA0, 1 and 2, and a data byte is written into the register. The GPIA then cancels the interrupt request.

5.3.10.4.4 Following the data transfer, the microprocessor sets IC17B, using line PB7, to give a logic 0 at IC18-12. This gives a logic 1 at IC18-11, which enables three bilateral switches in IC13 and connects the RFD line. The fourth switch in IC13 is disabled, thereby releasing IC12-18 from 0V. When the listening device asserts that it is ready for data, the GPIA loads the contents of the data-out register onto the bus and continues with the handshake routine.

5.3.10.4.5 When the data-out register has been read, the GPIA generates a further interrupt request. The microprocessor resets IC17B, using line PB6, giving a logic 1 at IC18-12 so that the RFD line is again broken at IC13. The data transfer and data transmission sequence is then repeated.

5.3.10.5 Serial Poll

5.3.10.5.1 The status byte register of the GPIA is normally updated approximately every 1 ms by the microprocessor. When the interface is addressed to talk following the receipt of the serial poll enable (SPE) message, the GPIA puts the status byte onto the bus without further action by the microprocessor.

5.3.10.5.2 When the serial poll is completed, the controller sends the serial poll disable (SPD) message, which is detected by IC26, IC7, IC18, and IC19. The resulting logic 1 at IC17B-3 clocks IC17B to the reset condition, and gives a logic 1 at IC18-12.

5.3.10.6 Data Transfer Between Microprocessors

5.3.10.6.1 Data transfer between microprocessors is made using the multiplexed data bus on both devices. Connections between the buses is made by means of a D-type latch, IC1 or IC2, depending on the direction of data transfer. All data transfers are initiated by the sending device. The first byte indicates the number of bytes to be transferred.

5.3.10.6.2 For data transfer to the GPIB microprocessor, the instrument's microprocessor sets SK1 pin 22 ($\overline{\text{GPIBIRQ}}$) low. This provides an interrupt request (IRQ) to the GPIB microprocessor via IC4. As part of the interrupt routine, IC8 is enabled and addressed to give an enabling signal for IC5A. The microprocessor reads the IRQ flag via IC5A and data bus line 7 to establish that the IRQ is from the instrument and not the GPIA.

5.3.10.6.3 The GPIB microprocessor prepares to receive data, and then enables and addresses IC8 to give a signal which clocks IC16B via IC20-6. The level set on line 0 of the data bus is transferred to IC16B-5, and forms the ready for data (RFD) signal to the instrument's microprocessor.

5.3.10.6.4 The instrument's microprocessor enables and addresses IC3 to give an enabling signal to IC5B, reads the RFD signal, puts the first data byte on the bus, and readdresses IC3 to give a clock signal which latches the data into IC1. It then addresses IC3 to give a clock signal for IC16A, so that the logic level set at IC16A-12 is transferred to IC16A-19 to form the data valid (DAV) signal to the GPIB microprocessor.

5.3.10.6.5 The GPIB microprocessor addresses IC8 to give a signal to enable IC5A, and reads the DAV signal via data bus line 6. It then cancels its RFD signal, addresses IC8 to give an output enable signal for IC1 (via IC20-8) and reads the data. A data accepted (DAC) signal is sent via IC2 and the RFD signal is reset. The instrument's microprocessor responds by cancelling its DAV signal and entering the next data byte into IC1. Data transfer continues in this manner until the required number of bytes have been received.

5.3.10.6.6 Data transfer from the GPIB microprocessor to the instrument's microprocessor follows a similar pattern. The IRQ signal is passed from port A line 0 via IC18 and IC4. The IRQ flag is read by the instrument's microprocessor during its interrupt routine, via IC5B (enabled by an output from IC3). The IRQ signal is cancelled by the instrument's microprocessor setting data bus line 0 to logic 0 and then addressing IC3 to clock IC17A. The resulting logic 0 at IC17B-9 disables IC18-4.

5.3.10.6.7 During data transfer from the GPIB interface to the instrument, the RFD signal is passed via IC16A and IC5A, the DAV signal via IC16B and IC5B, the DAC signal via IC1, and the data via IC2.

SECTION 6 MAINTENANCE

INTRODUCTION

1 This section provides information on the following:

(1) Required test equipment

(2) Dismantling and reassembly

(3) Diagnostic special functions

(4) Troubleshooting Flowcharts

(5) Instrument setup (either post-repair or after specification check failure)

(6) Overall specification check

REQUIRED TEST EQUIPMENT

2 A complete list of required test equipment is provided in Table 6.1 on the next page. Equipment needed for specific procedures is indicated at the beginning of each set of instructions.

3 Particular models of specific equipment types are recommended in some categories. However, equipment having operating characteristics equivalent to or better than those listed may be substituted. The procedures described in this section are general ones and based on the use of the test equipment recommended. Some modification to the procedures may be necessary if substituted equipment is used.

TABLE 6.1

Required Test Equipment

Item	Minimum Use Specification	Recommended Equipment
1. Frequency Standard	10 MHz; accuracy better than ± 3 parts in 10^{10}	Racal-Dana 9475
2. Oscilloscope with an X1 probe	50 MHz bandwidth	TEK 454
3. Digital Multimeter	Frequency range of DC to 5 kHz; input level of 20 mV to 6V	Racal-Dana 5001
4. Signal Generator	10 kHz to 1.3 GHz	Racal-Dana 9087
5. Audio Generator	Frequency range of 10 Hz to 5 kHz; output level of 30 mV into 50 ohms	Racal-Dana 9083
6. Pulse Generator	Single positive-going pulse with +0.8V low and +2.8V high levels (TTL limit-level)	Racal-Dana P25
7. BNC T-Connector	50 ohms	
8. Connector Lead	50-ohm coaxial cable with BNC connectors, length between 0.80m and 1m	
9. Coaxial Load	BNC connector, 50 ohms	
10. GPIB Controller		HP85
11. GPIB Analyzer		RD488

DISMANTLING AND REASSEMBLY

Introduction

4 Instructions for dismantling or reassembling the counter are limited to those areas where special care is required or difficulty may be experienced.

REMOVAL OF COVERS

WARNING: DANGEROUS AC VOLTAGES ARE EXPOSED WHEN THE COVERS ARE REMOVED WITH THE INSTRUMENT CONNECTED TO AN AC SUPPLY. TURN THE INSTRUMENT OFF AND DISCONNECT THE SUPPLY PLUG FROM THE REAR PANEL PRIOR TO ANY DISMANTLING OR REASSEMBLY.

Instrument Covers

5 Complete the following procedure:

(1) Disconnect the AC power cord from the rear panel.

(2) Unscrew the two phillips head screws from each rear corner-foot.

(3) Slide the top cover 1/2 inch towards the rear panel and lift off. The bottom cover slides off in the same manner.

6 To replace the covers, reverse the above procedure. Ensure that the tongues of the covers fit under the edges of the frame on the front panel.

Front Panel

7 Complete the following procedure:

(1) Remove the instrument covers.

(2) Remove the side panels by sliding toward rear of instrument.

(3) Turning counterclockwise, remove the clamping collars from the front-panel BNC connectors for INPUTs A and B. Use the special wrench (Racal-Dana P/N 14-1586).

(4) Remove the two screws securing the handles to the side frame at both sides of the counter.

(5) Remove the two screws securing the front panel to side frame which are exposed by removing the handles.

(6) Ease the front panel forward.

(7) To completely disconnect the front panel, unplug PL1 and PL2 from the motherboard.

(8) Remove the two screws securing the on/off switch to the front panel.

(9) Disconnect the coaxial lead from the back of Input C (Option 41 only).

8 To replace the front panel, reverse the above procedure. Pass the POWER button through its aperture in the front panel and reconnect the Input C amplifier (Option 41 only) before securing the front panel.

Rear Panel

9 Complete the following procedure:

(1) Remove the instrument covers.

(2) Disconnect the following flying leads between motherboard and rear panel:

(a) PL14 to Reference Oscillator

(b) Q6, Q12, and Q8 to transistors on the rear panel

(c) TP1 and TP2 to Gate Output

(3) Remove the screws securing the rear panel to the side frame which are exposed by removing the rear-corner feet.

(4) Ease the rear panel away from the counter, disconnecting the BNC mounting board assembly from the motherboard at PL19 and PL20.

(5) Remove the nut and crinkle washer securing the rectifier bridge D11 to the rear panel.

(6) Disconnect the green/yellow ground lead connecting the rear panel stud to the power input plug.

10 To replace the rear panel, reverse the above procedure.

LETHAL VOLTAGE

WARNING: THE GROUNDING OF THE COUNTER'S EXTERNAL METALWORK DEPENDS UPON THE INTEGRITY OF THE CONNECTION BETWEEN THE REAR PANEL STUD AND POWER INPUT PLUG. ENSURE THAT THE GREEN/YELLOW GROUND LEAD IS PROPERLY CONNECTED DURING REASSEMBLY.

Input C Amplifier Board (Option 41)

11 Complete the following procedure:

(1) Remove the counter's top cover.

(2) Remove the two screws securing the Input C PCB to the support plate.

(3) Disconnect the coaxial lead from the Ch. C PCB.

(4) Gently pull the amplifier PCB assembly upwards until the board disconnects from the motherboard at SK7. This permits access to both sides of the board for servicing.

12 To replace the amplifier PCB assembly, reverse the above procedure.

Display Board

13 Complete the following procedure:

(1) Remove the instrument covers.

(2) Remove the counter's front panel.

(3) Remove the seven screws securing the display board to the front panel, then remove the board itself.

14 To replace the display board, reverse the above procedure.

DIAGNOSTIC SPECIAL FUNCTIONS

15 Refer to Section 3 and Table 3.13 for a full description of the counter's special functions. Listed below in Table 6.2 are those special function numbers for use during maintenance and calibration. (Check mode must be selected.)

TABLE 6.2

Diagnostic Special Functions

Function Number	Function
70	Basic 10 MHZ check (default)
71	Front-panel LED check
72	Start TEC (Timing Error Correction) short, continuous calibration. Application of a 100 ns pulse with TEC count shown on display
73	Start TEC long, continuous calibration. Application of a 200 ns pulse with TEC count shown on display
74	Stop TEC short calibration
75	Stop TEC long calibration
76	Input A and B DAC check with continuous ramping through the DACs
77	Input A relay check
78	Input B relay check

16 **Special Function 70**

Special function 70 is the default state of its decade. It provides measurement of the 10 MHz internal frequency standard and verifies operation of the microprocessor system, MCC1, MCC2 and the TEC.

17 **Special Function 71**

Special function 71 exercises all the LEDs, except STANDBY, GATE, TRIG A, TRIG B, REM, ADDR and SRQ, at approximately 0.5 Hz. If the GPIB interface (Option 55) is fitted, the REM, ADDR and SRQ indicators light.

18 **Special Functions 72, 73, 74 and 75**

Special functions 72, 73, 74 and 75 should only be used for diagnostic purposes at an ambient temperature of 23,C ±2,C.

19 The TEC long counts must be 800 ±220. The TEC short counts must be in the range (0.5 x long count) +20 to -40. Counts outside these ranges indicate a malfunction of the TEC circuit.

20 **Special Function 76**

Special function 76 continuously exercises the DACs in both Channel A and Channel B through the range -5.1V to +5.1V. The waveform can be monitored at the trigger output pins on the rear panel.

21 **Special Function 77**

Special function 77 continuously tests the relays associated with Channel A input: X1/X10 attenuators, 50Ω /1MΩ input impedance, DC/AC coupling, FILTER and COM A. The 10 MHz STD OUTPUT from the rear panel BNC must be connected to the Channel A input.

22 **Special Function 78**

Special function 78 continuously tests the relays associated with Channel B input: X1/X10 attenuators, 50Ω /1MΩ input impedance and DC/AC coupling. The 10 MHz STD OUTPUT from the rear panel BNC must be connected to the Channel B input.

23 **Special Function Error Codes**

Listed below in Table 6.3 are displayed error codes for the diagnostic Special Functions.

TABLE 6.3

Special Function Error Codes

Display	Special Function Number	Error
Er 50	70 or 71	Basic CHECK mode error
Er 51	77	Input A relay check: X10/X1
Er 52		Input A relay check: 50 /1m
Er 53		Input A relay check: DC/AC
Er 54		Input A relay check: FILTER
Er 55		Input A relay check: COM A
Er 56	78	Input B relay check: X10/X1
Er 57		Input B relay check: 50 /1m
Er 58		Input B relay check: DC/AC

TROUBLESHOOTING FLOWCHARTS

Introduction

24 Refer to Fig 6.1 (A-F) and 6.2 for main counter and GPIB troubleshooting flowcharts. They are designed to facilitate the user in tracing specific 1994 faults and failures to their sources.

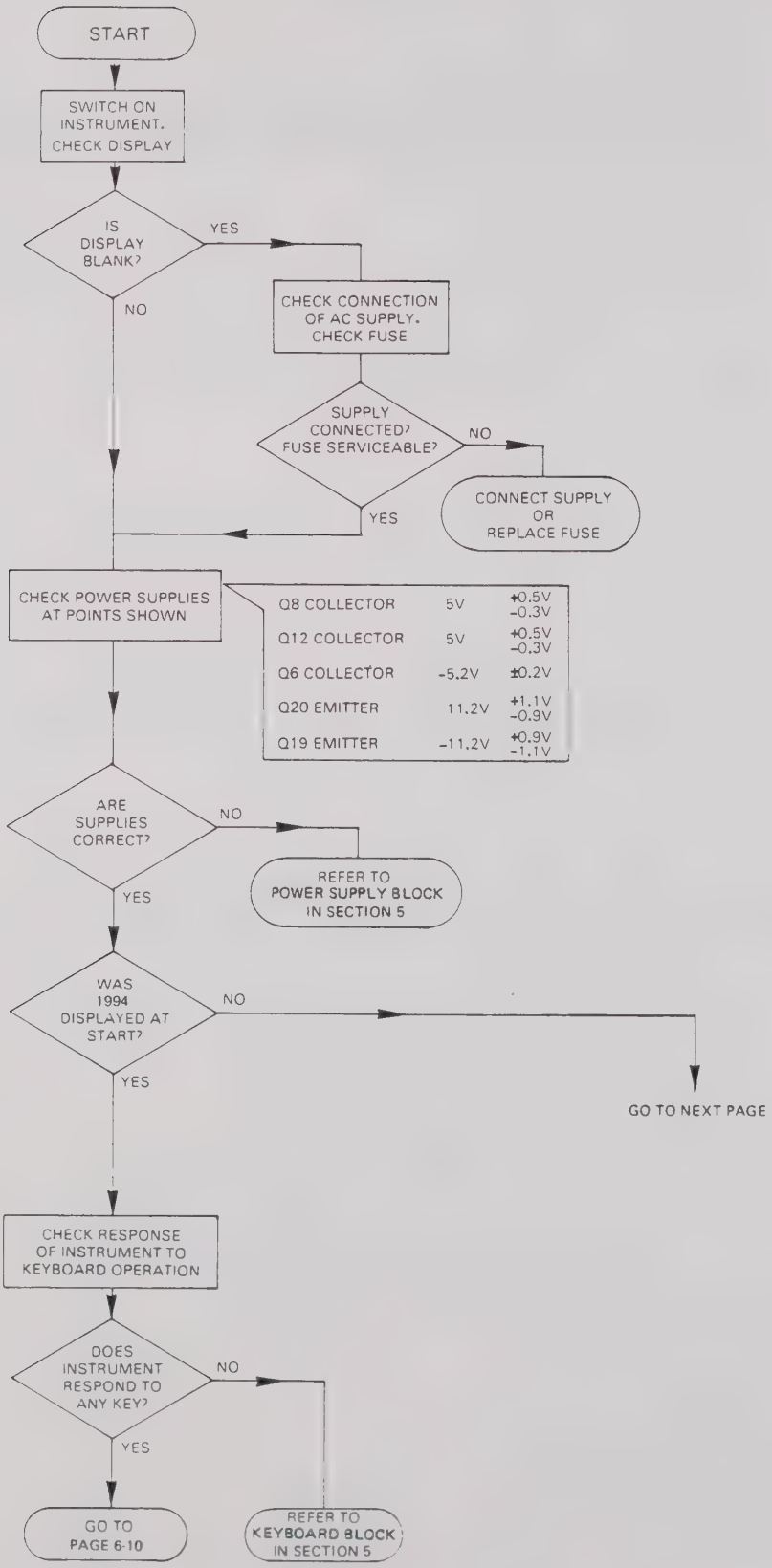


Figure 6.1 - Fault Finding Flowchart - Part 1

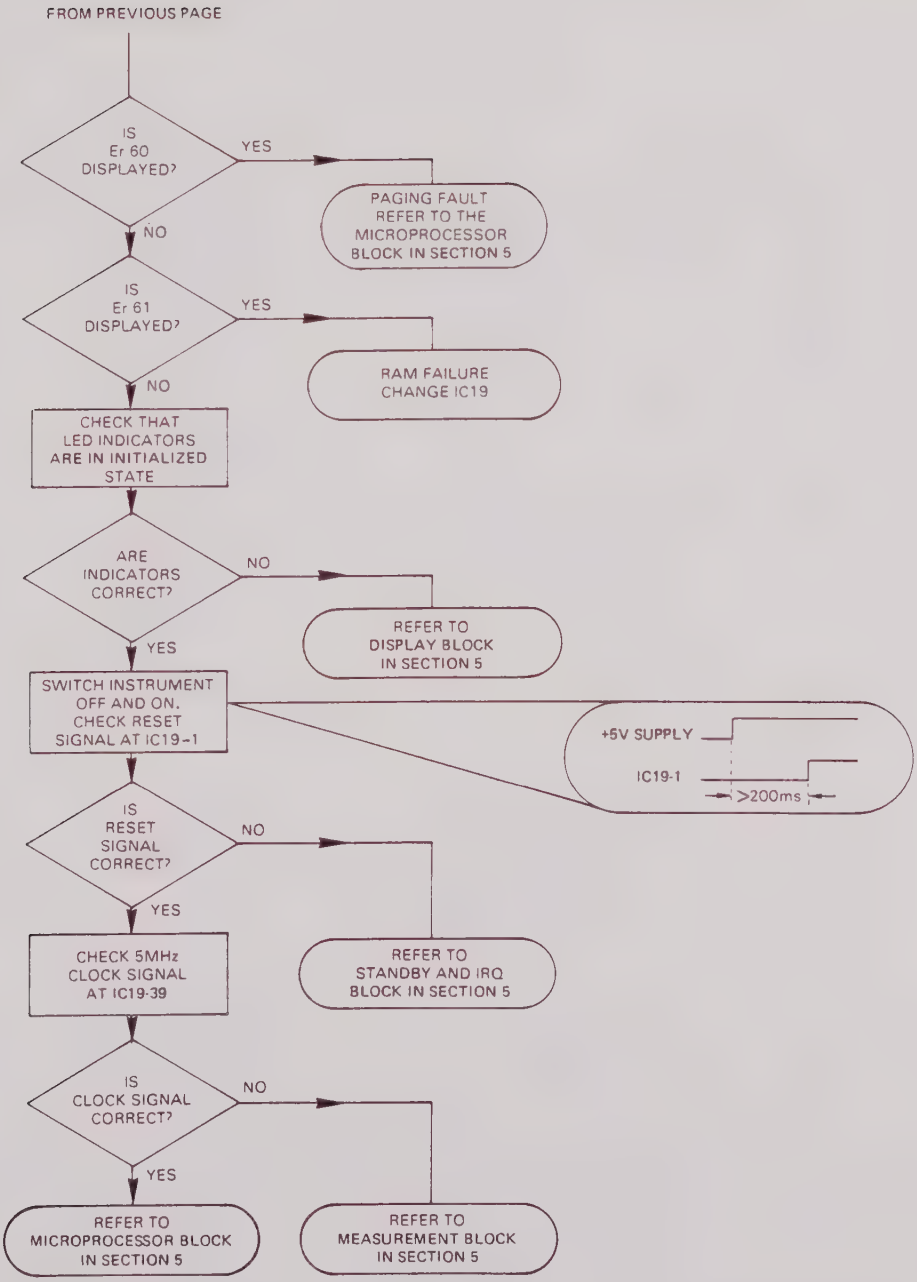


Figure 6.1 – Fault Finding Flowchart – Part 1 (Cont'd)

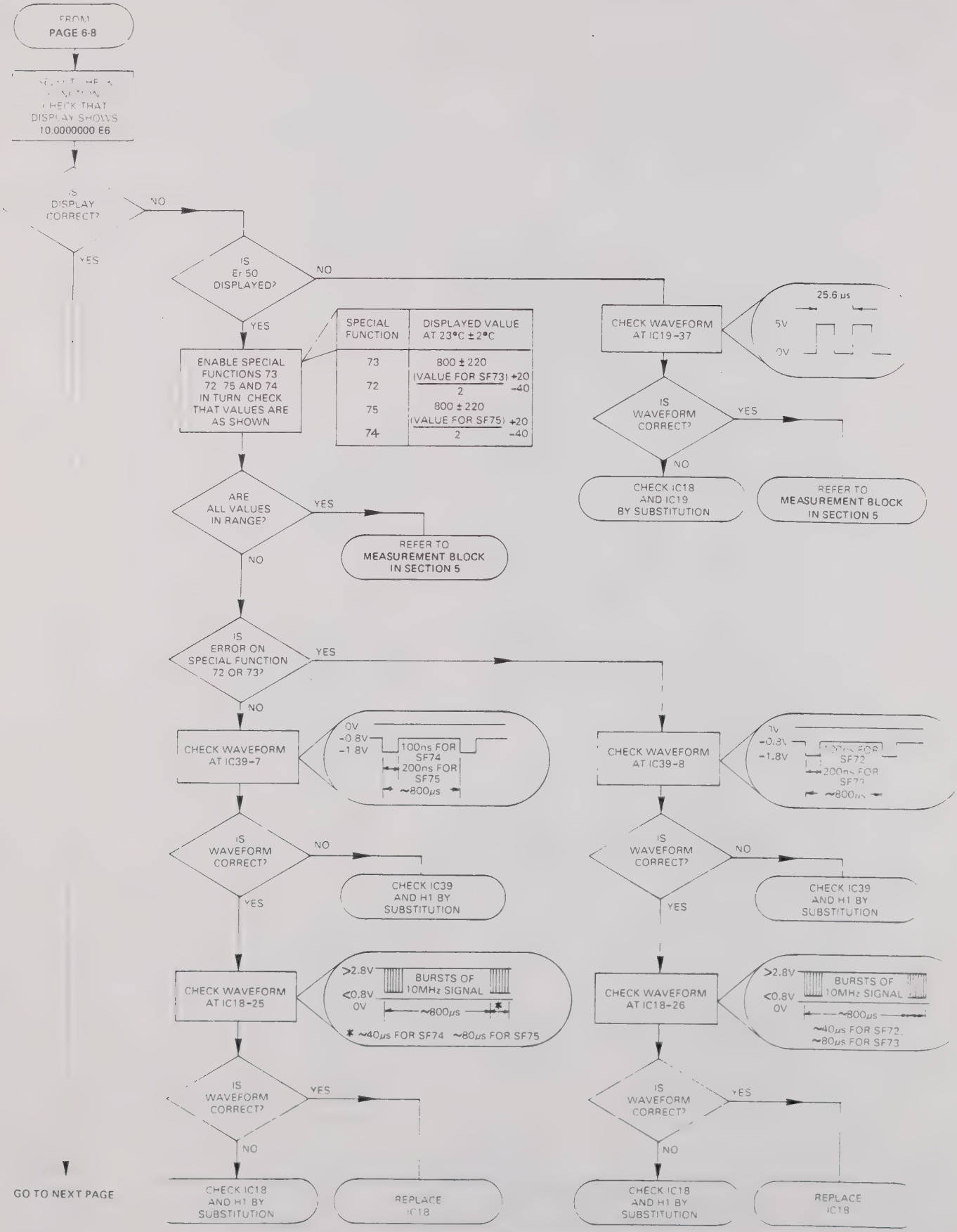


Figure 6.1 - Fault Finding Flowchart - Part 2

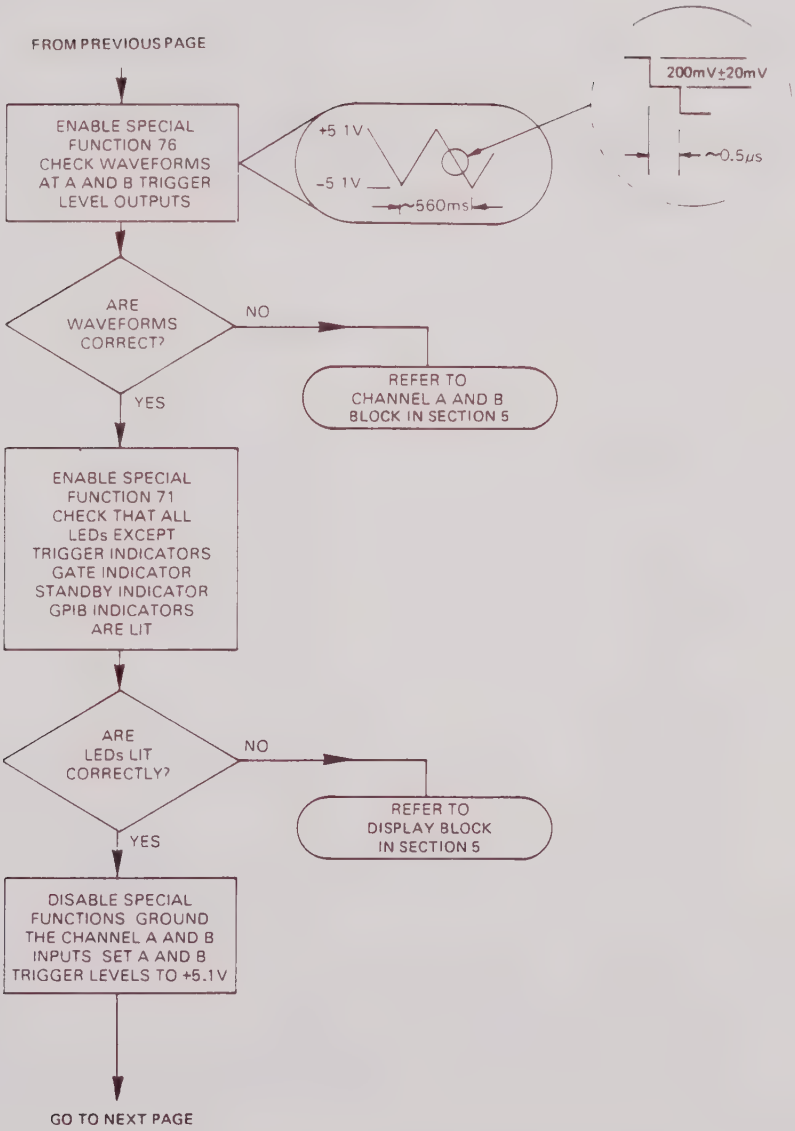

FROM PREVIOUS PAGE
ENABLE SPECIAL FUNCTION 76 CHECK WAVEFORMS AT A AND B TRIGGER LEVEL OUTPUTS
+5 1V
-5 1V
~560ms
200mV±20mV
~0.5µs
ARE WAVEFORMS CORRECT?
NO
REFER TO CHANNEL A AND B BLOCK IN SECTION 5
YES
ENABLE SPECIAL FUNCTION 71 CHECK THAT ALL LEDs EXCEPT TRIGGER INDICATORS GATE INDICATOR STANDBY INDICATOR GPIB INDICATORS ARE LIT
ARE LEDs LIT CORRECTLY?
NO
REFER TO DISPLAY BLOCK IN SECTION 5
YES
DISABLE SPECIAL FUNCTIONS GROUND THE CHANNEL A AND B INPUTS SET A AND B TRIGGER LEVELS TO +5.1V
GO TO NEXT PAGE

Figure 6.1 - Fault Finding Flowchart - Part 3

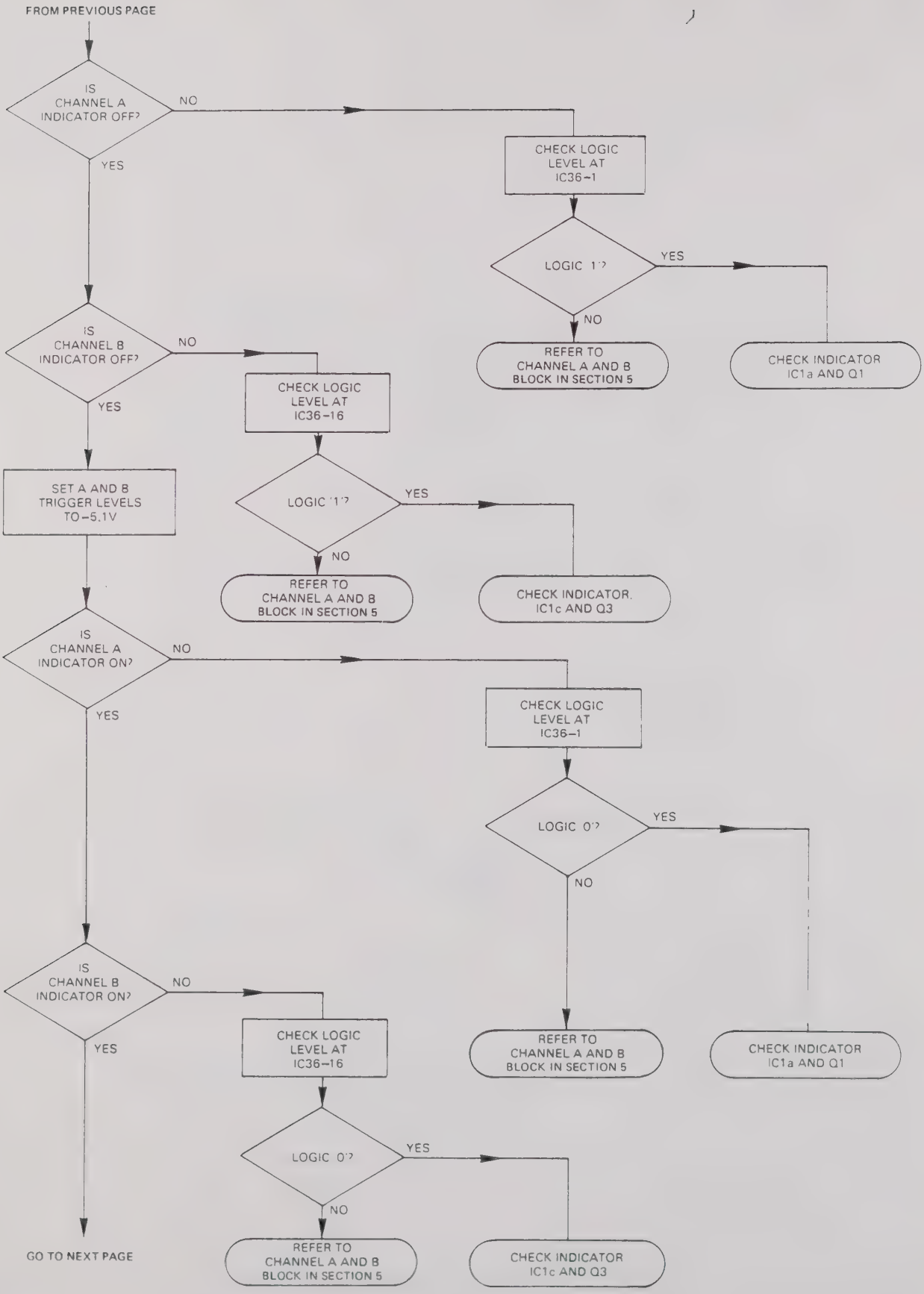


Figure 6.1 - Fault Finding Flowchart - Part 3 (Cont'd)

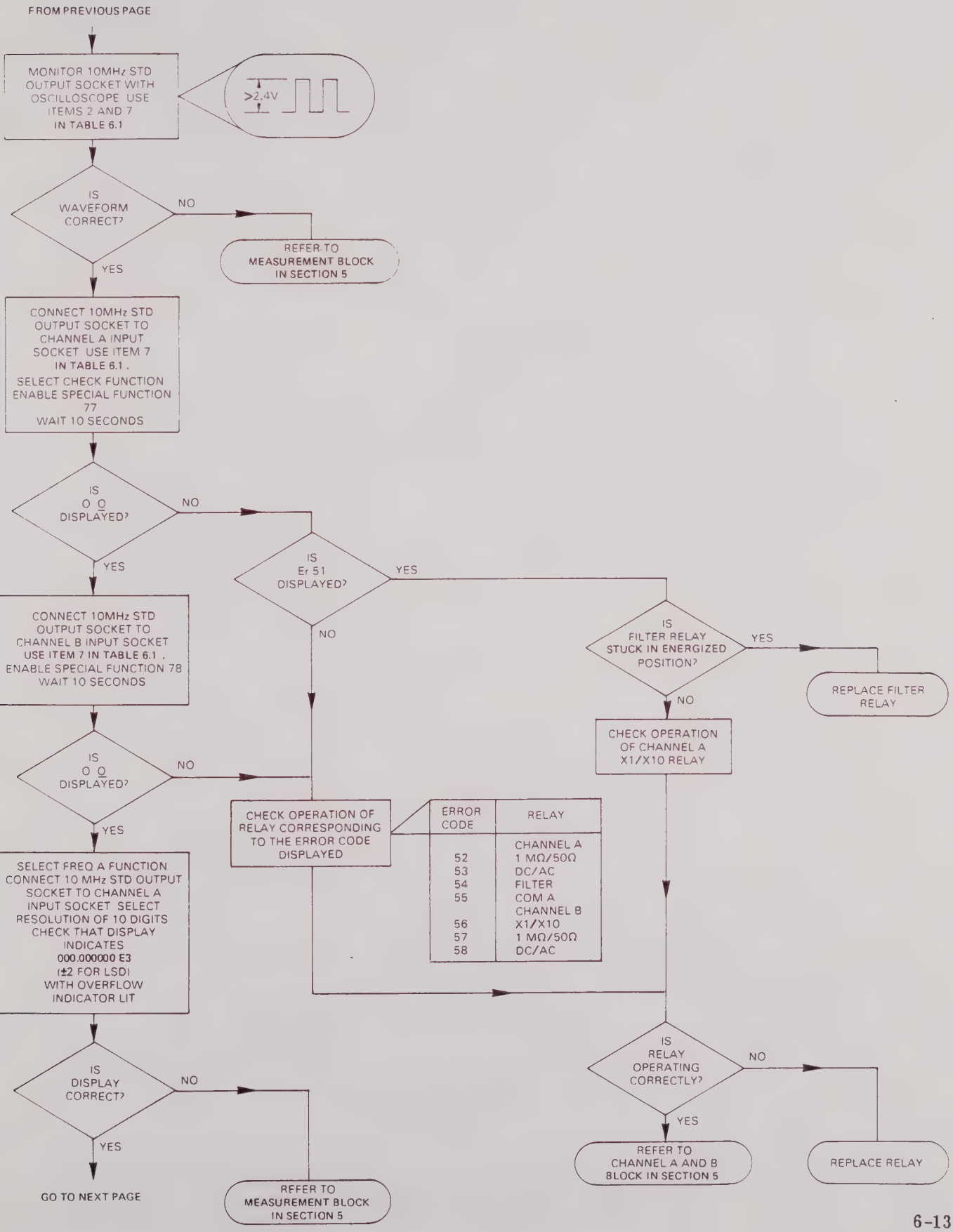

FROM PREVIOUS PAGE
MONITOR 10MHz STD OUTPUT SOCKET WITH OSCILLOSCOPE USE ITEMS 2 AND 7 IN TABLE 6.1
>2.4V
IS WAVEFORM CORRECT?
NO
YES
REFER TO MEASUREMENT BLOCK IN SECTION 5
CONNECT 10MHz STD OUTPUT SOCKET TO CHANNEL A INPUT SOCKET USE ITEM 7 IN TABLE 6.1 . SELECT CHECK FUNCTION ENABLE SPECIAL FUNCTION 77 WAIT 10 SECONDS
IS O O DISPLAYED?
NO
YES
IS Er 51 DISPLAYED?
YES
NO
IS FILTER RELAY STUCK IN ENERGIZED POSITION?
YES
REPLACE FILTER RELAY
NO
CHECK OPERATION OF CHANNEL A X1/X10 RELAY
CONNECT 10MHz STD OUTPUT SOCKET TO CHANNEL B INPUT SOCKET USE ITEM 7 IN TABLE 6.1 . ENABLE SPECIAL FUNCTION 78 WAIT 10 SECONDS
IS O O DISPLAYED?
NO
YES
CHECK OPERATION OF RELAY CORRESPONDING TO THE ERROR CODE DISPLAYED
ERROR CODE
RELAY
52 CHANNEL A 1 MΩ/50Ω
53 DC/AC
54 FILTER
55 COM A
CHANNEL B
56 X1/X10
57 1 MΩ/50Ω
58 DC/AC
SELECT FREQ A FUNCTION CONNECT 10 MHz STD OUTPUT SOCKET TO CHANNEL A INPUT SOCKET SELECT RESOLUTION OF 10 DIGITS CHECK THAT DISPLAY INDICATES 000.000000 E3 (±2 FOR LSD) WITH OVERFLOW INDICATOR LIT
IS DISPLAY CORRECT?
NO
YES
GO TO NEXT PAGE
REFER TO MEASUREMENT BLOCK IN SECTION 5
IS RELAY OPERATING CORRECTLY?
NO
YES
REFER TO CHANNEL A AND B BLOCK IN SECTION 5
REPLACE RELAY

Figure 6.1 – Fault Finding Flowchart – Part 4

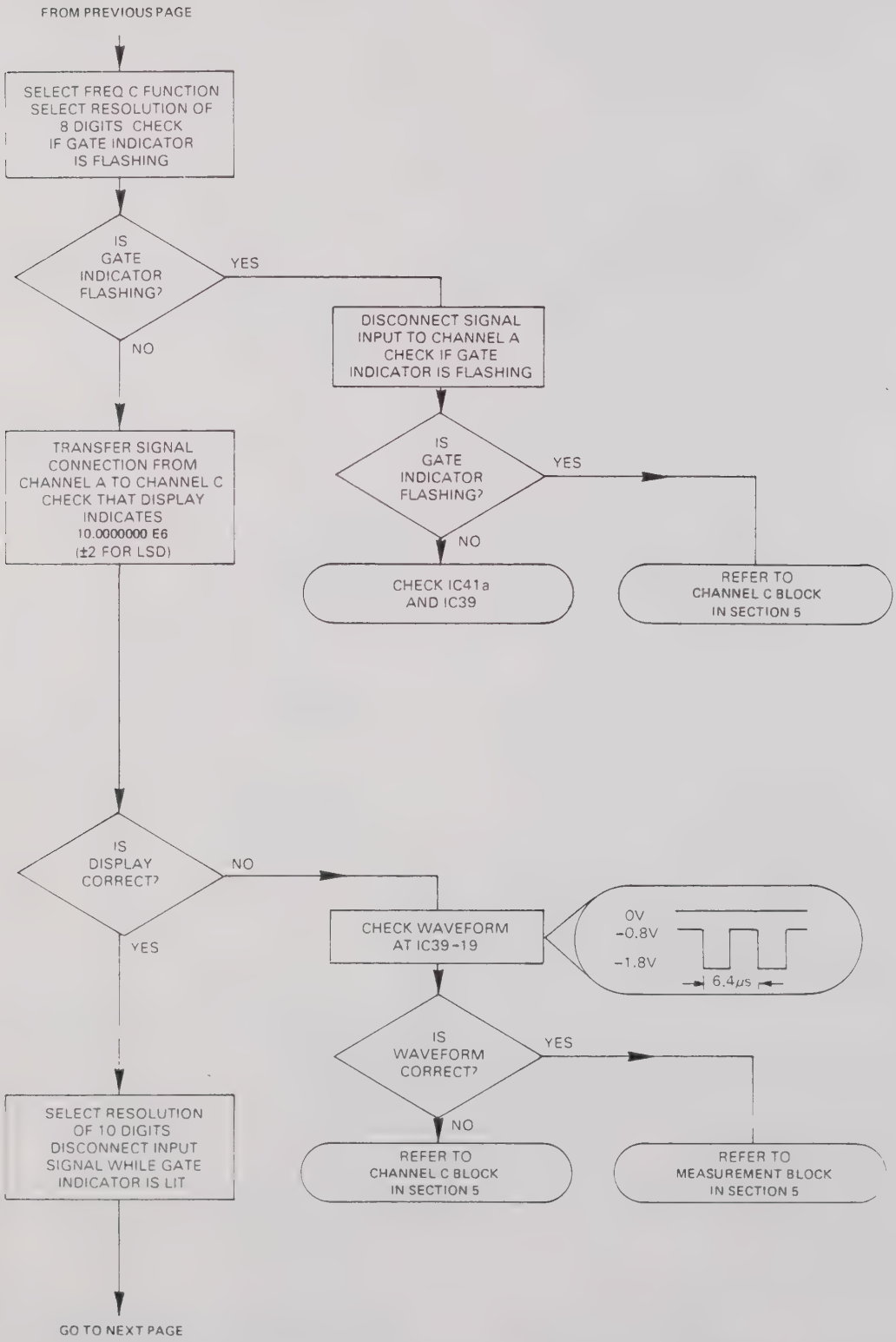

FROM PREVIOUS PAGE
SELECT FREQ C FUNCTION SELECT RESOLUTION OF 8 DIGITS CHECK IF GATE INDICATOR IS FLASHING
IS GATE INDICATOR FLASHING?
YES
NO
DISCONNECT SIGNAL INPUT TO CHANNEL A CHECK IF GATE INDICATOR IS FLASHING
IS GATE INDICATOR FLASHING?
YES
NO
CHECK IC41a AND IC39
REFER TO CHANNEL C BLOCK IN SECTION 5
TRANSFER SIGNAL CONNECTION FROM CHANNEL A TO CHANNEL C CHECK THAT DISPLAY INDICATES 10.0000000 E6 (±2 FOR LSD)
IS DISPLAY CORRECT?
NO
YES
CHECK WAVEFORM AT IC39-19
0V
-0.8V
-1.8V
6.4μs
IS WAVEFORM CORRECT?
YES
NO
REFER TO CHANNEL C BLOCK IN SECTION 5
REFER TO MEASUREMENT BLOCK IN SECTION 5
SELECT RESOLUTION OF 10 DIGITS DISCONNECT INPUT SIGNAL WHILE GATE INDICATOR IS LIT
GO TO NEXT PAGE

Figure 6.1 - Fault Finding Flowchart - Part 5

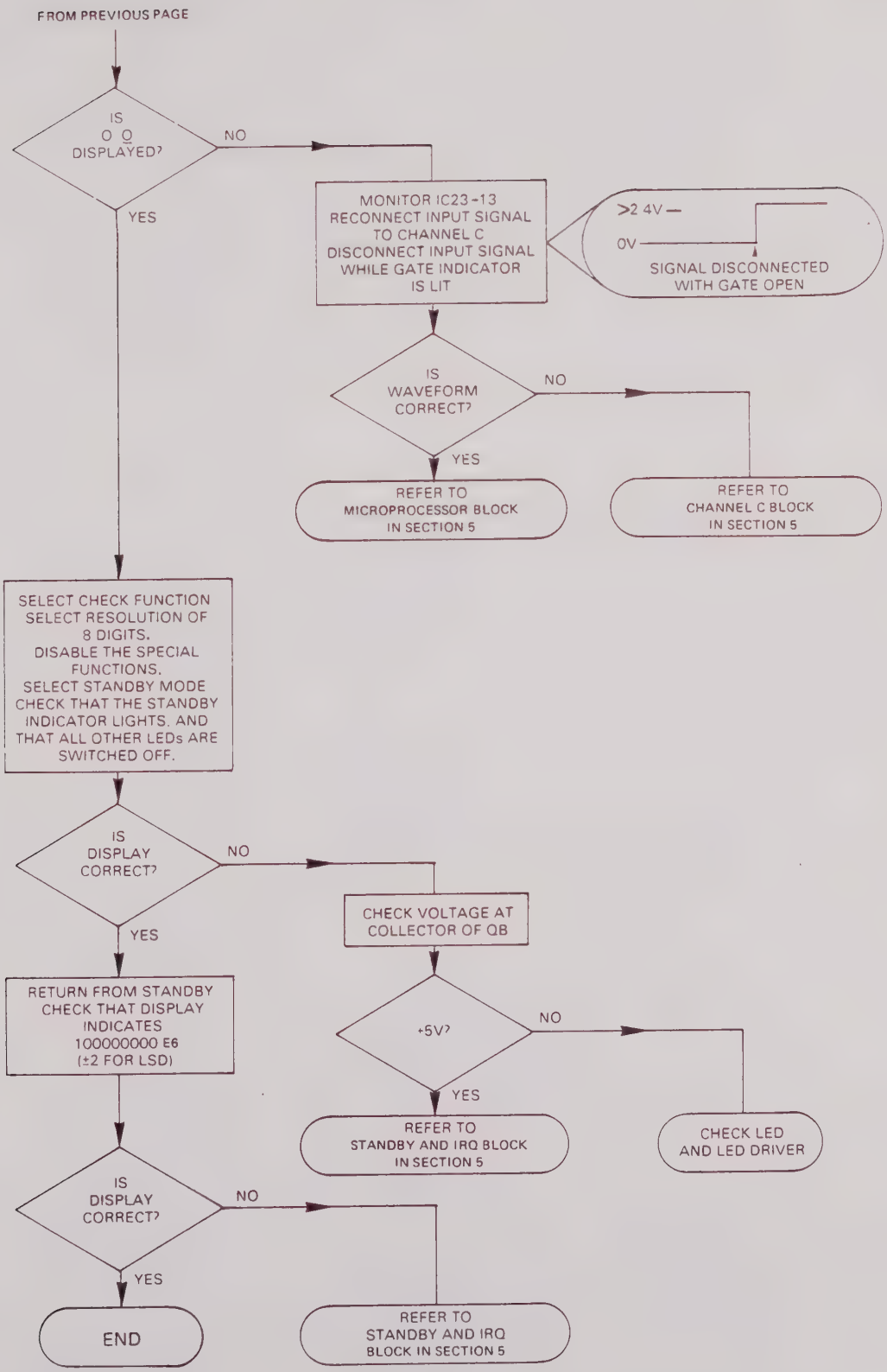


Figure 6.1 - Fault Finding Flowchart - Part 5 (Cont'd)

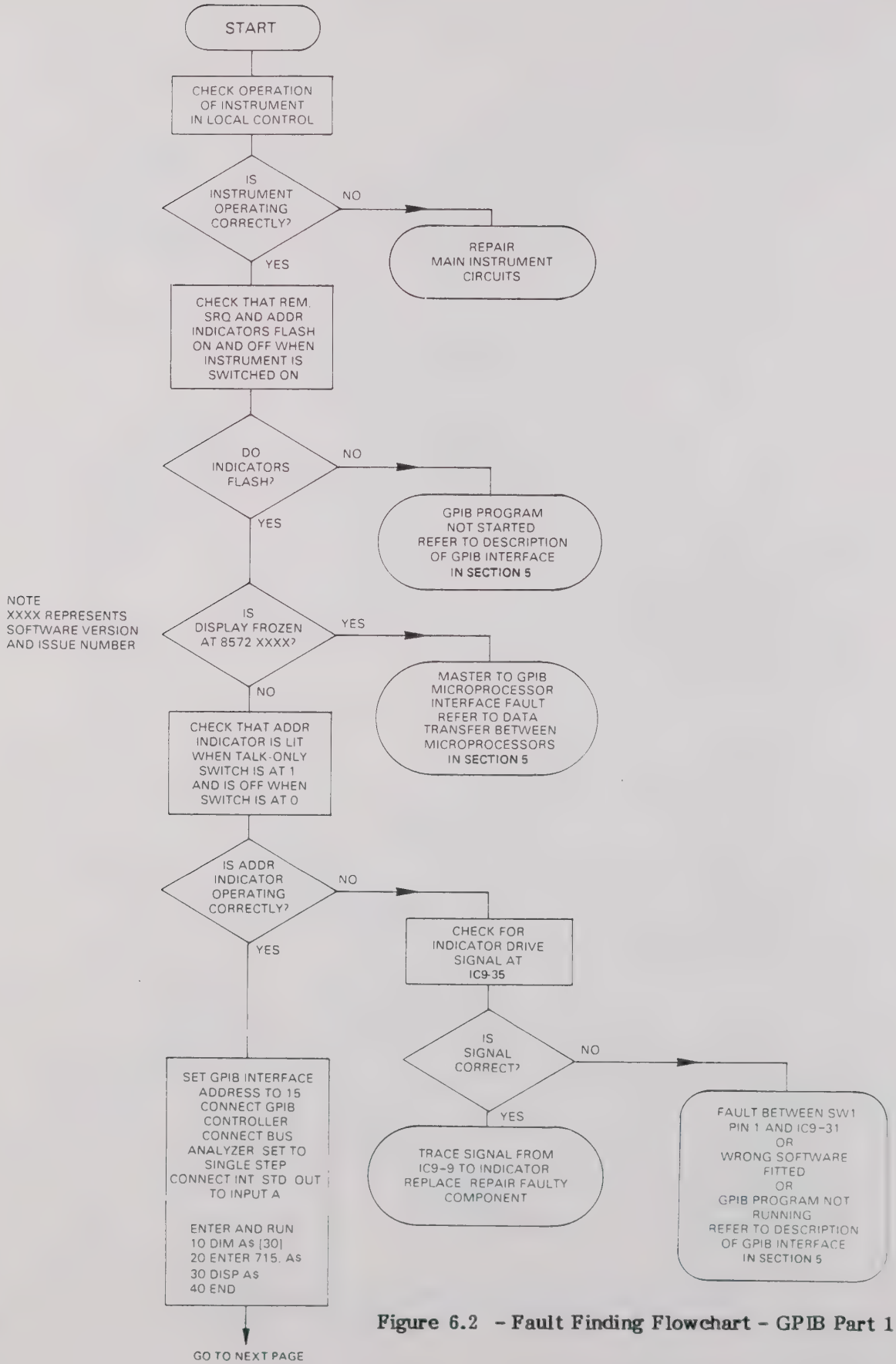

START
CHECK OPERATION OF INSTRUMENT IN LOCAL CONTROL
IS INSTRUMENT OPERATING CORRECTLY?
NO
REPAIR MAIN INSTRUMENT CIRCUITS
YES
CHECK THAT REM, SRQ AND ADDR INDICATORS FLASH ON AND OFF WHEN INSTRUMENT IS SWITCHED ON
DO INDICATORS FLASH?
NO
GPIB PROGRAM NOT STARTED REFER TO DESCRIPTION OF GPIB INTERFACE IN SECTION 5
YES
NOTE XXXX REPRESENTS SOFTWARE VERSION AND ISSUE NUMBER
IS DISPLAY FROZEN AT 8572 XXXX?
YES
MASTER TO GPIB MICROPROCESSOR INTERFACE FAULT REFER TO DATA TRANSFER BETWEEN MICROPROCESSORS IN SECTION 5
NO
CHECK THAT ADDR INDICATOR IS LIT WHEN TALK-ONLY SWITCH IS AT 1 AND IS OFF WHEN SWITCH IS AT 0
IS ADDR INDICATOR OPERATING CORRECTLY?
NO
CHECK FOR INDICATOR DRIVE SIGNAL AT IC9-35
YES
IS SIGNAL CORRECT?
NO
YES
SET GPIB INTERFACE ADDRESS TO 15
CONNECT GPIB CONTROLLER
CONNECT BUS ANALYZER SET TO SINGLE STEP
CONNECT INT STD OUT TO INPUT A
ENTER AND RUN
10 DIM A$ [30]
20 ENTER 715, A$
30 DISP A$
40 END
TRACE SIGNAL FROM IC9-9 TO INDICATOR REPLACE REPAIR FAULTY COMPONENT
FAULT BETWEEN SW1 PIN 1 AND IC9-31
OR
WRONG SOFTWARE FITTED
OR
GPIB PROGRAM NOT RUNNING
REFER TO DESCRIPTION OF GPIB INTERFACE IN SECTION 5
GO TO NEXT PAGE

Figure 6.2 - Fault Finding Flowchart - GPIB Part 1

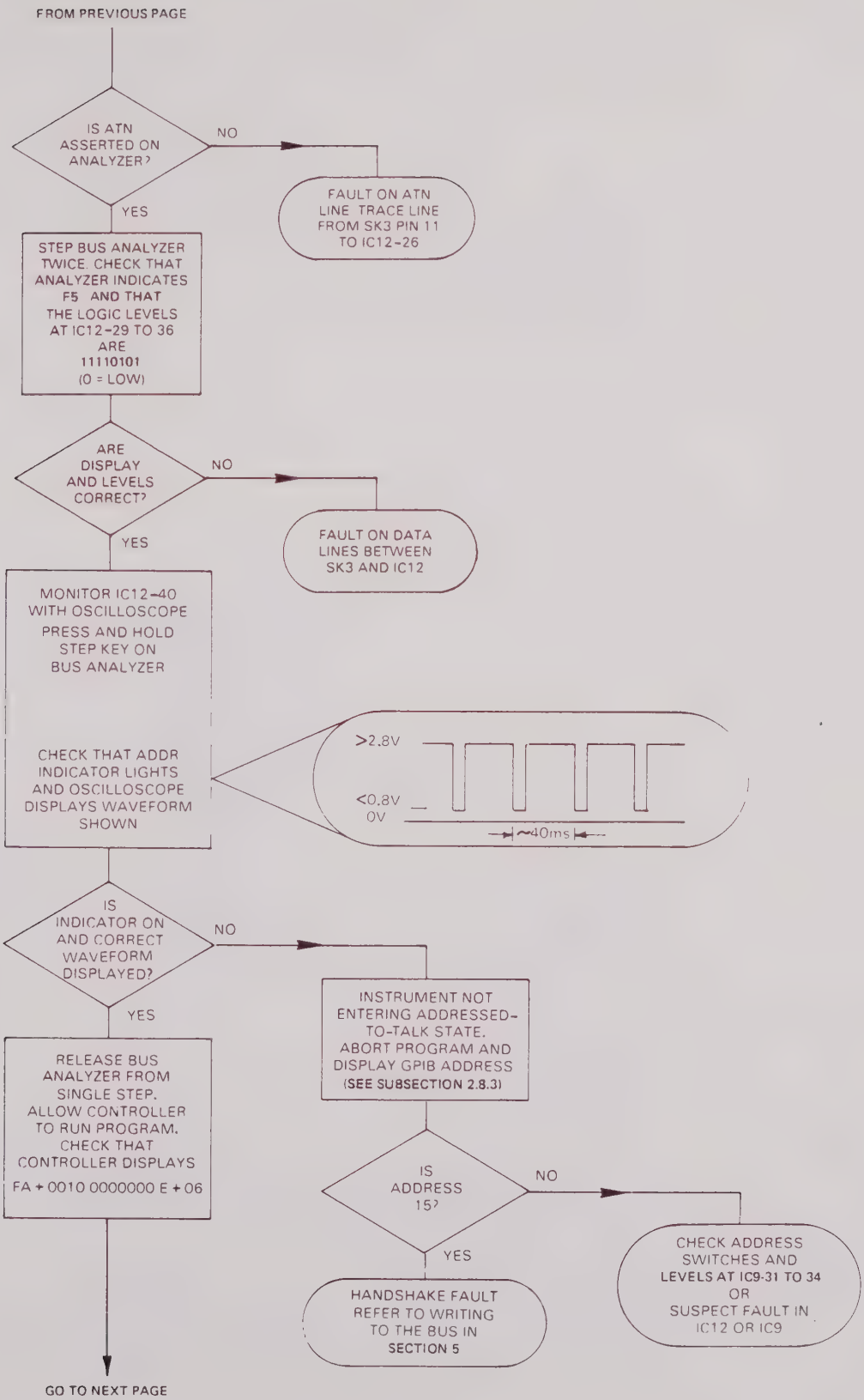

FROM PREVIOUS PAGE
IS ATN ASSERTED ON ANALYZER?
NO
FAULT ON ATN LINE TRACE LINE FROM SK3 PIN 11 TO IC12-26
YES
STEP BUS ANALYZER TWICE. CHECK THAT ANALYZER INDICATES F5 AND THAT THE LOGIC LEVELS AT IC12-29 TO 36 ARE 11110101 (0 = LOW)
ARE DISPLAY AND LEVELS CORRECT?
NO
FAULT ON DATA LINES BETWEEN SK3 AND IC12
YES
MONITOR IC12-40 WITH OSCILLOSCOPE
PRESS AND HOLD STEP KEY ON BUS ANALYZER
CHECK THAT ADDR INDICATOR LIGHTS AND OSCILLOSCOPE DISPLAYS WAVEFORM SHOWN
>2.8V
<0.8V
0V
~40ms
IS INDICATOR ON AND CORRECT WAVEFORM DISPLAYED?
NO
INSTRUMENT NOT ENTERING ADDRESSED-TO-TALK STATE. ABORT PROGRAM AND DISPLAY GPIB ADDRESS (SEE SUBSECTION 2.8.3)
YES
RELEASE BUS ANALYZER FROM SINGLE STEP. ALLOW CONTROLLER TO RUN PROGRAM. CHECK THAT CONTROLLER DISPLAYS FA + 0010 0000000 E + 06
IS ADDRESS 15?
NO
CHECK ADDRESS SWITCHES AND LEVELS AT IC9-31 TO 34 OR SUSPECT FAULT IN IC12 OR IC9
YES
HANDSHAKE FAULT REFER TO WRITING TO THE BUS IN SECTION 5
GO TO NEXT PAGE

Figure 6.2 - Fault Finding Flowchart - GPIB Part 2

FROM PREVIOUS PAGE

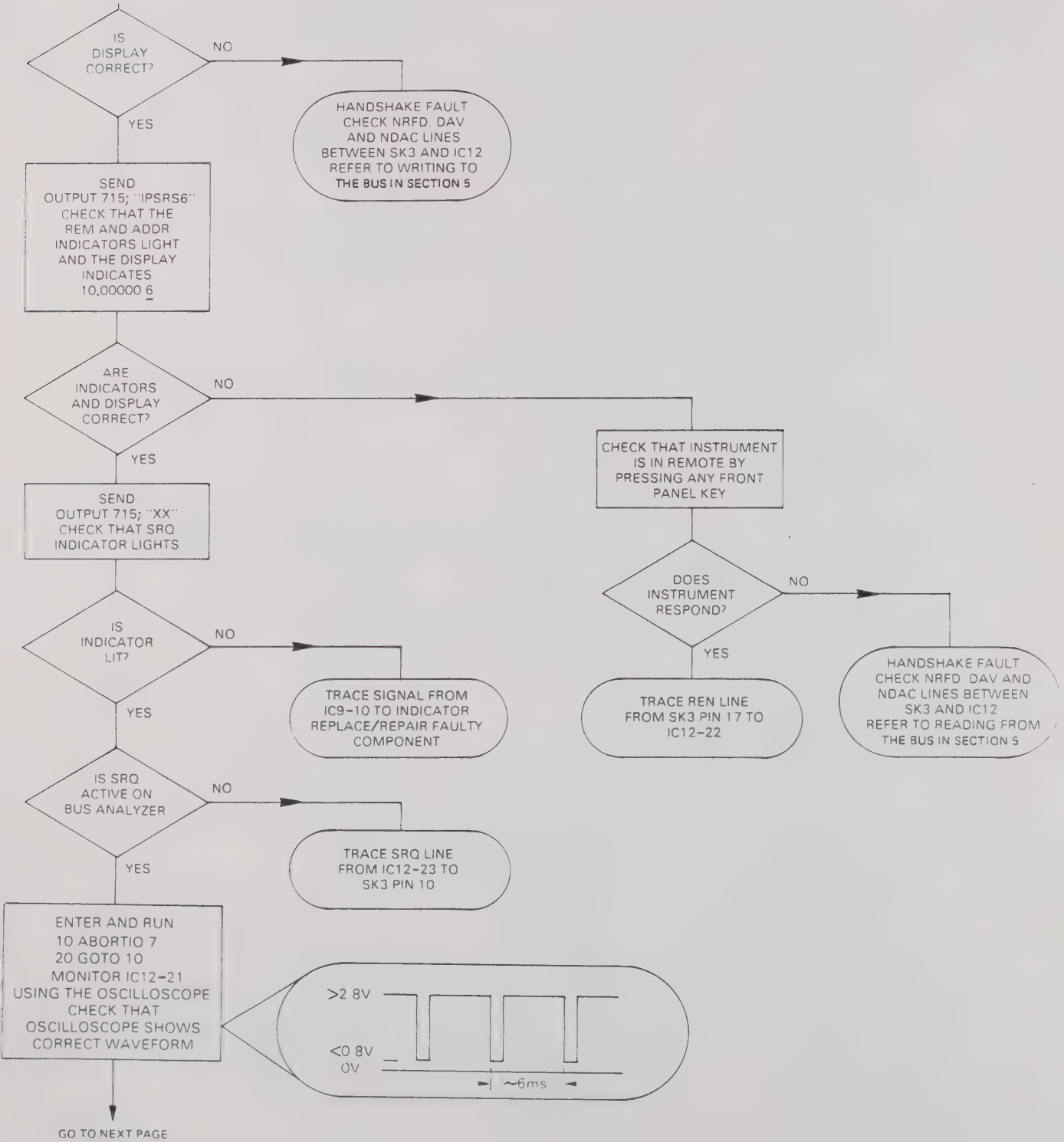

IS DISPLAY CORRECT?
NO
HANDSHAKE FAULT CHECK NRFD, DAV AND NDAC LINES BETWEEN SK3 AND IC12 REFER TO WRITING TO THE BUS IN SECTION 5
YES
SEND OUTPUT 715; "IPSRS6" CHECK THAT THE REM AND ADDR INDICATORS LIGHT AND THE DISPLAY INDICATES 10,00000 6
ARE INDICATORS AND DISPLAY CORRECT?
NO
CHECK THAT INSTRUMENT IS IN REMOTE BY PRESSING ANY FRONT PANEL KEY
YES
SEND OUTPUT 715; "XX" CHECK THAT SRQ INDICATOR LIGHTS
DOES INSTRUMENT RESPOND?
NO
HANDSHAKE FAULT CHECK NRFD DAV AND NDAC LINES BETWEEN SK3 AND IC12 REFER TO READING FROM THE BUS IN SECTION 5
YES
TRACE REN LINE FROM SK3 PIN 17 TO IC12-22
IS INDICATOR LIT?
NO
TRACE SIGNAL FROM IC9-10 TO INDICATOR REPLACE/REPAIR FAULTY COMPONENT
YES
IS SRQ ACTIVE ON BUS ANALYZER
NO
TRACE SRQ LINE FROM IC12-23 TO SK3 PIN 10
YES
ENTER AND RUN 10 ABORTIO 7 20 GOTO 10 MONITOR IC12-21 USING THE OSCILLOSCOPE CHECK THAT OSCILLOSCOPE SHOWS CORRECT WAVEFORM
>2 8V
<0 8V
0V
~6ms
GO TO NEXT PAGE

Figure 6.2 - Fault Finding Flowchart - GPIB Part 3

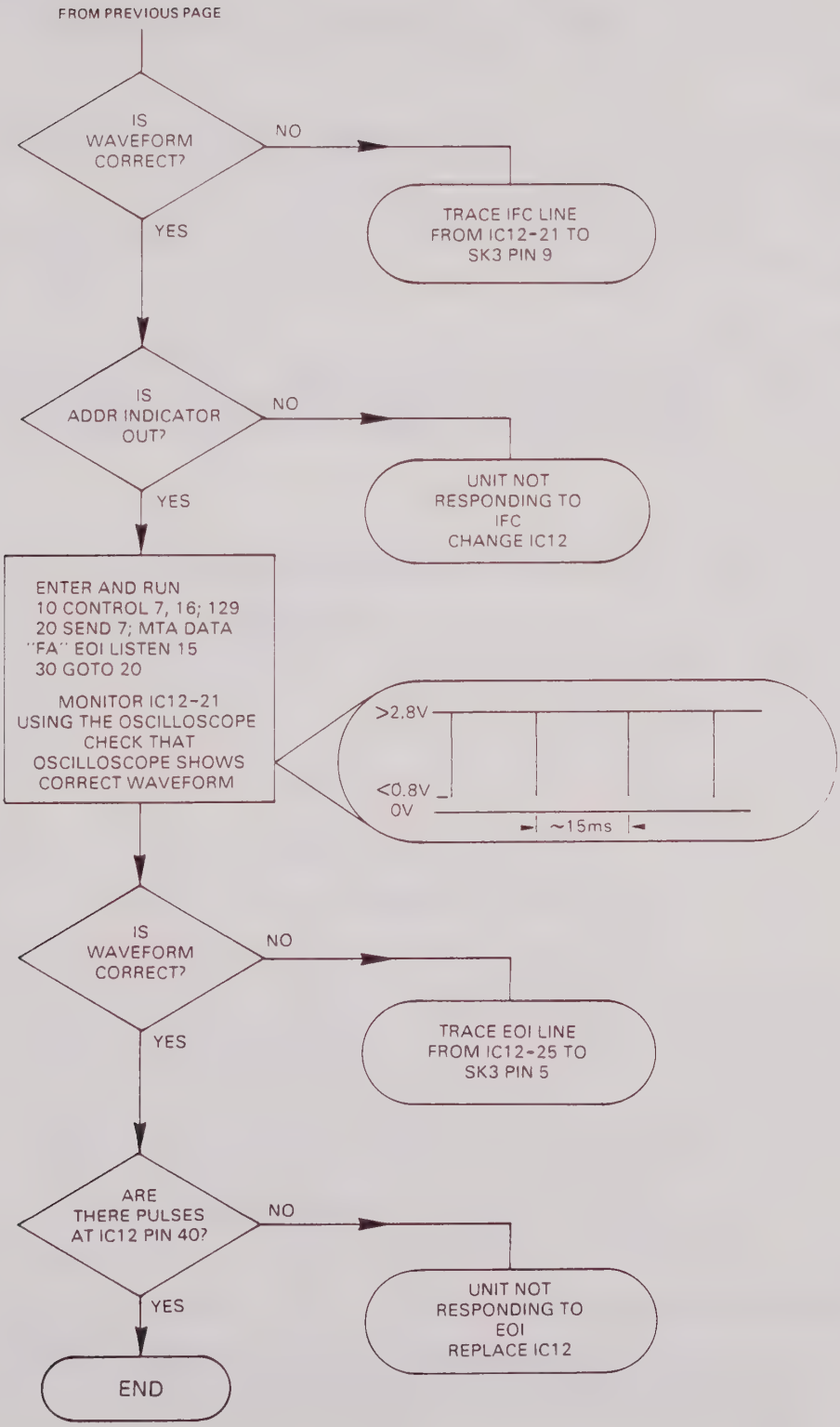


Figure 6.2 - Fault Finding Flowchart - GPIB Part 4

25 COUNTER SETUP (POST-REPAIR/POST-SPECIFICATION CHECK FAILURE)

Introduction

After repair, appropriate setup procedures as decribed in this subsection should be performed prior to initiating an overall specification check. These procedures should also be used if the counter fails a routine specification check.

26 Ambient temperature must be maintained at 23°C ± 2°C throughout these procedures.

LETHAL VOLTAGE

WARNING: THESE PROCEDURES REQUIRE THE COUNTER TO BE OPERATED WITH COVERS REMOVED. DANGEROUS AC VOLTAGES ARE EXPOSED UNDER THESE CONDITIONS.

Input A System

27 Required test equipment includes a signal generator (see Table 6.1; Item 4).

28 First, set resistors R149 fully counterclockwise and R192 to its midposition. R192 is located inside the screened module (access holes provided) as shown in Fig 6.3.

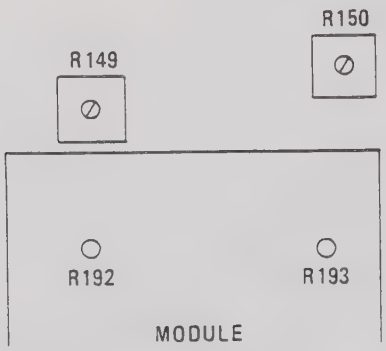


Fig. 6.3 Location of R149 and R192

29 Complete the following procedure:

(1) Turn on the counter. Select 50 ohms for Input A and function FREQ A.

(2) Press the RESOLUTION key five times until 000 is displayed.

(3) Connect the test equipment as shown in Fig 6.4.

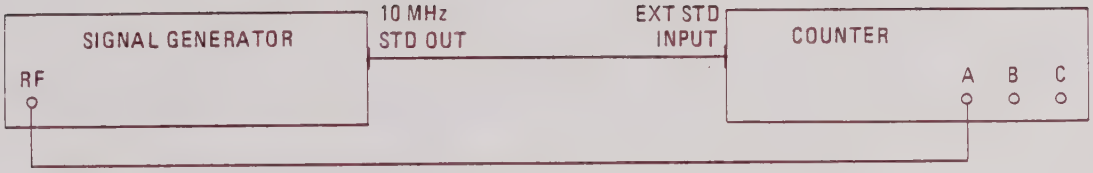


Fig. 6.4 Connections for Input A System Adjustment

(5) Verify that the EXT STD LED (front panel) is lit, and that INPUT A TRIG LED is flashing.

(4) Set the signal generator output to 100 MHz at a level of 3.0 mV r.m.s.

(6) Adjust R192 to obtain the most stable display of 100.0 E 6 ±0.1 E 6, with the GATE LED flashing.

NOTE:

Care is required when adjusting R192. The display indication is random when R192 is set to either side of its correct position.

30 Complete the following procedure:

(1) Turn off the RF output of the signal generator.

(2) Press the RESOLUTION ↑ key five times until 00000000 is displayed.

NOTE:

Disregard any noisy readings that may be experienced.

(3) Turn on the RF output of the signal generator.

(4) Increase the generator's output to 13 mV r.m.s.

(5) Adjust R149 slowly clockwise until the display just becomes unstable. Turn R149 slowly counterclockwise until the display is just stable, showing 100.000000 E 6±0.000001 E 6.

(6) Reduce the generator's output to 7 mV r.m.s. Verify that the GATE LED stops flashing. If flashing continues, repeat steps 4 through 6.

(7) Turn off the counter and disconnect the test equipment.

Input B System

31 Required test equipment includes a signal generator (see Table 6.1; Item 4).

32 First, set resistors R150 fully counterclockwise and R193 to its midposition. R193 is located inside the screened module (access holes provided) as shown in Fig 6.5.

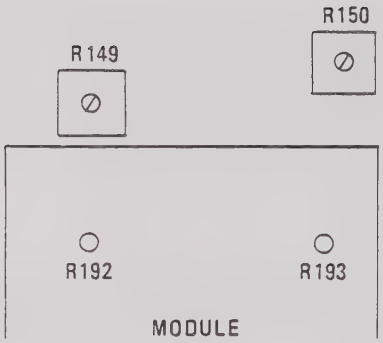


Fig 6.5 Location of R150 and R193

33 Complete the following procedure:

(1) Turn on the counter. Select 50 ohms for Input B and function FREQ A.

(2) Press key sequence

[2] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF].

(3) Press the RESOLUTION ↓ key five times until 000 is displayed.

(4) Connect the test equipment as shown in Fig. 6.6.

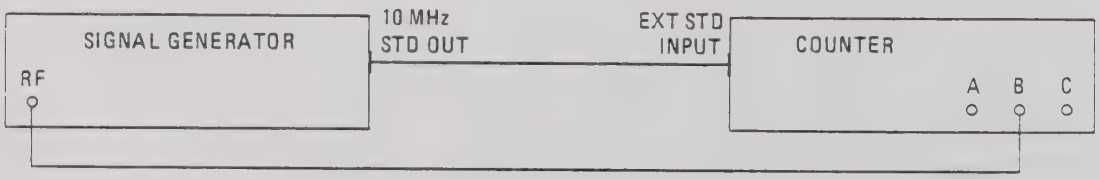


Fig 6.6 Connections for Input B System Adjustment

(5) Set the signal generator output to 100 MHz at a level of 3.0 mV r.m.s.

(6) Verify that the EXT STD LED (front panel) is lit, and that INPUT B TRIG LED is flashing.

(7) Adjust R193 to obtain the most stable display of 100.0 E 6 ±0.1 E 6, with the GATE LED flashing.

NOTE:

Care is required when adjusting R193. The display indication is random when R193 is set to either side of its correct position.

34 Complete the following procedure:

(1) Turn off the RF output of the signal generator.

(2) Press the RESOLUTION ↑ key five times until 00000000 is displayed.

NOTE:

Disregard any noisy readings that may be experienced.

(3) Turn on the RF output of the signal generator.

(4) Increase the generator's output to 13 mV r.m.s.

(5) Adjust R150 slowly clockwise until the display just becomes unstable. Turn R150 slowly counterclockwise until the display is just stable, showing 100.000000 E 6 ±0.000001 E 6.

(6) Reduce the generator's output to 7 mV r.m.s. Verify that the GATE LED stops flashing. If flashing continues, repeat steps 4 through 6.

(7) Turn off the counter and disconnect the test equipment.

Input C Assembly (Option 41 only)

35 Required test equipment includes a signal generator and connector lead (see Table 6.1; Items 4 and 8).

36 Connect the test equipment as shown in Fig. 6.7.

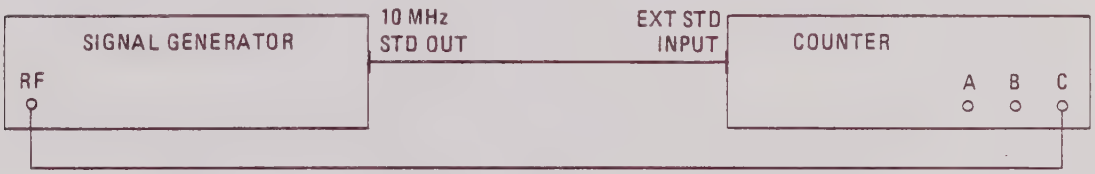


Fig. 6.7 Connections for Input C Assembly Adjustment

37 Complete the following procedure:

(1) Set resistor R27 on the Input C Assembly board fully clockwise.

(2) Turn on the counter. Select function FREQ C. Verify that the EXT STD LED (front panel) is lit.

(3) Set the signal generator output to 1 GHz at a level of 5.0 mV r.m.s.

(4) Adjust R27 slowly counterclockwise until the GATE LED just starts flashing and the display shows 1000.00000 E 6 ±0.00001 E 6.

(5) Turn off the RF output of the signal generator. Decrease the output level to 4.5 mV r.m.s.

(6) Turn on the RF output of the signal generator. Verify that the 1994 is not counting. If it is, repeat steps 3 through 6.

(7) Turn off the counter and disconnect the test equipment.

Internal Frequency Standard - Routine Calibration

38 Required test equipment includes a frequency standard (see Table 6.1; Item 1).

NOTE:

If either Option 04A or 04E ovenized frequency standard is installed, allow the counter to warm up for one hour (switched to standby, if required) before making any adjustment.

39 Complete the following procedure:

(1) Turn the counter on. Select function FREQ A. Verify that 00000000 is displayed. If Option 04E is installed, press the RESOLUTION ↑ key until 000000000 is displayed.

(2) Connect the test equipment as shown in Fig 6.8.

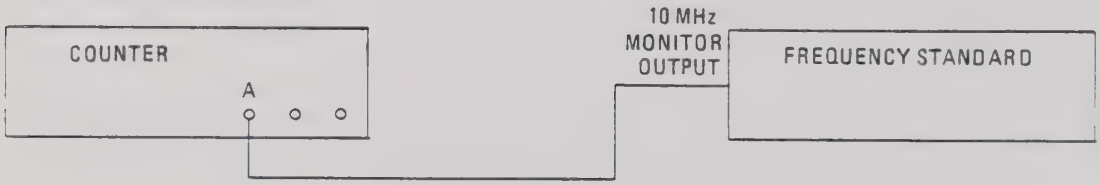


Fig 6.8 Connections for Internal Frequency Standard Adjustment

(3) Press key sequence

[1] [0] [EXP] [6] [SHIFT] [STORE] [X] .

(4) Press key sequence

[SHIFT] [RECALL] [X] .

Verify that 10.000000 E 6 is displayed.

(5) Press [CONTINUE] and key sequence [SHIFT] [R-X/Z] .

(6) Adjust the internal frequency standard as close as possible to 10 MHz, using the FREQ STD ADJUST aperture on the rear panel. The accuracy limits are shown in Table 6.4. Verify that the value displayed is within these limits.

TABLE 6.4

Internal Frequency Standard Accuracy

Frequency Standard	Limits # Digits	Limits Exp.
Standard oscillator	± 16	0
Option 04A	± 3	0
Option 04E	± 10	-3

(7) Turn off the counter and disconnect the test equipment.

OVERALL SPECIFICATION CHECK

Introduction

40 Satisfactory completion of the following performance verification procedures (PVPs) will confirm that the counter is functional and meets its specification. Before beginning the specification check, ensure that the counter successfully passes the functional check provided in Section 2, par. 2.9 of this manual. The PVPs should be completed in the order given.

41 The following conditions must be kept throughout the specification check:

(1) The counter must be operated from an AC supply.

(2) The line voltage must be within the indicated range of the line voltage selector.

(3) The instrument covers must be installed.

(4) The ambient temperature must be 23°C ± 2°C.

(5) The power supply to the frequency standard must be uninterrupted.

42 The counter should be allowed to warm up for one hour (switched to standby, if required) before beginning the specification check.

Input A Sensitivity PVP

43 Required equipment includes a digital multimeter, signal generator, audio generator, and BNC T-Connector (see Table 6.1; Items 3, 4, 5, and 7).

44 Complete the following procedure:

(1) Turn on the counter. Select 50 ohms for Input A.

(2) Connect the test equipment as shown Fig 6.9A. Verify that the EXT STD LED lights.

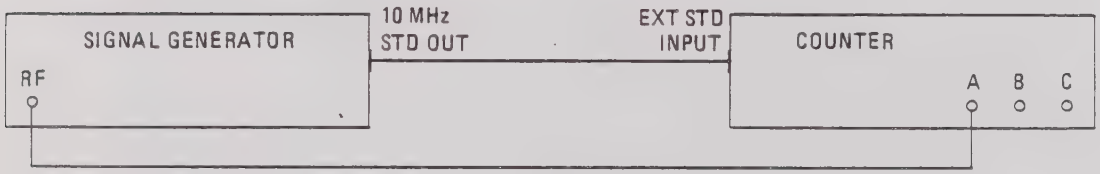


Fig 6.9A Connections for Input A Sensitivity PVP (I)

(3) Set, in turn, the signal generator output to the frequencies shown in Table 6.5A. Set the counter's resolution to the corresponding values.

TABLE 6.5A

Input A Sensitivity (I)

Frequency	1994 Resolution	Signal Level
160 MHz	8 digits	40 mV
100 MHz	8 digits	20 mV
10 MHz	7 digits	20 mV
100 kHz	5 digits	20 mV

(4) For each selected frequency, determine the minimum input level to the counter that provides stable counting. Verify that these minimum levels do not exceed those shown in the table.

(5) Disconnect the test equipment.

45 Complete the following procedure:

(1) Connect the test equipment as shown in Fig. 6.9B.

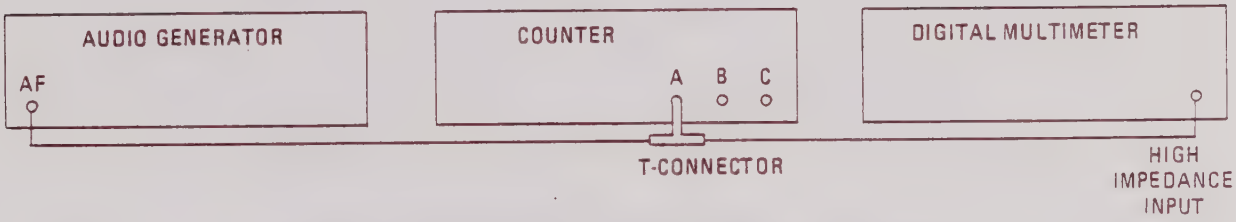


Fig. 6.9B Connections for Input A Sensitivity PVP (II)

(2) Set, in turn, the audio generator output to the frequencies shown in Table 6.5B. Set the counter's resolution to the corresponding values.

TABLE 6.5B

Input A Sensitivity (II)

Frequency	Counter Resolution	Signal Level
5 kHz	3 Digits	20 mV
10 Hz	3 Digits	20 mV

(3) For each selected frequency, determine the minimum input level to the counter that provides stable counting. Verify that these minimum levels do not exceed those shown in the table.

(4) Disconnect the test equipment.

Input B Sensitivity PVP

46 Required equipment includes a digital multimeter, signal generator, audio generator, and BNC T-Connector (see Table 6.1; Items 3, 4, 5, and 7).

47 Complete the following procedure:

(1) Select 50 ohms for Input B.

(2) Connect the test equipment as shown in Fig. 6.10A. Verify that the EXT STD LED lights.

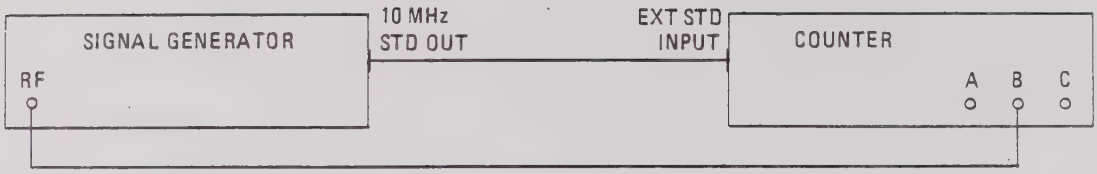


Fig. 6.10A Connections for Input B Sensitivity PVP (I)

(3) Press the key sequence

2 1 SHIFT STORE SF SHIFT SF .

(4) Set, in turn, the signal generator output at the frequencies shown in Table 6.6A. Set the counter's resolution to the corresponding values.

TABLE 6.6A

Input B Sensitivity (I)

Frequency	Counter Resolution	Signal Level
100 MHz	8 digits	20 mV
10 MHz	7 digits	20 mV
100 kHz	5 digits	20 mV

(5) For each selected frequency, determine the minimum input level to the counter that provides stable counting. Verify that these minimum levels do not exceed those shown in the table.

(6) Disconnect the test equipment.

48 Complete the following procedure:

(1) Connect the test equipment as shown in Fig. 6.10B.

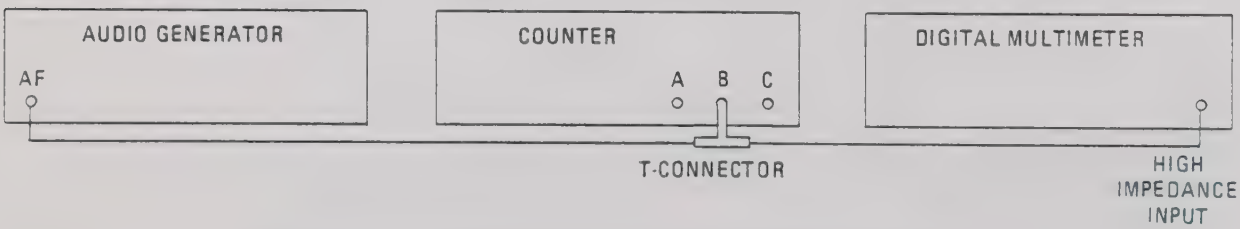


Fig. 6.10B Connections for Input B Sensitivity PVP (II)

(2) Set, in turn, the audio generator output to the frequencies shown in Table 6.6B. Set the counter's resolution to the corresponding values.

TABLE 6.6B

Input B Sensitivity (II)

Frequency	Counter Resolution	Signal Level
5 kHz	3	20 mV
10 Hz	3	20 mV

(3) For each selected frequency, determine the minimum input level to the counter that provides stable counting. Verify that these minimum levels do not exceed those shown in the table.

(4) Press the key sequence

[2] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF] .

(5) Turn off and disconnect the test equipment.

Input C Sensitivity PVP (Option 41 only)

49 Required equipment includes a signal generator and connector lead (see Table 6.1; Items 4 and 8).

50 Complete the following procedure:

(1) Connect the test equipment as shown in Fig. 6.11.

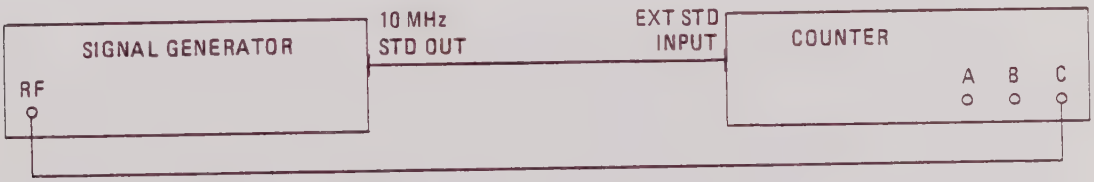


Fig. 6.11 Connections for Input C Sensitivity PVP

(2) Select function FREQ C.

(3) Set, in turn, the signal generator output to the frequencies shown in Table 6.7. Set the counter's resolution to the corresponding values.

TABLE 6.7

Input C Sensitivity

Frequency	Counter Resolution	Signal Level
40 MHz	8 digits	10 mV
100 MHz	8 digits	10 mV
500 MHz	8 digits	10 mV
1.0 GHz	9 digits	10 mV
1.3 GHz	9 digits	50 mV

(4) For each selected frequency, determine the minimum input level to the counter that provides stable counting. Verify that these minimum levels do not exceed those shown in the table.

(5) Disconnect the test equipment.

External Standard Input Sensitivity PVP

51 Required equipment includes a signal generator (see Table 6.1; Item 4).

52 Complete the following procedure:

(1) Connect the signal generator output to the EXT. STD. INPUT socket on the rear panel of the counter.

(2) Set the signal generator output to 10 MHz at a level of 10 mV.

(3) Slowly increase the signal level until the counter's EXT STD LED lights steadily.

(4) Verify that the signal level does not exceed 70 mV r.m.s.

(5) Disconnect the signal generator.

10 MHz Standard Output Level PVP

53 Required test equipment includes an oscilloscope, BNC T-Connector, and coaxial load (see Table 6.1; Items 2, 7, and 9).

54 Complete the following procedure:

(1) Connect the test equipment as shown in Fig. 6.12.

Fig. 6.12 Connections for 10 MHz Standard Output Level PVP

(2) Verify that the peak-to-peak amplitude of the displayed waveform is not less than 0.5V. Verify that the mark-space ratio is between 30:70 and 70:30.

(3) Disconnect the test equipment.

Minimum Time Interval PVP

55 Required test equipment includes a signal generator (see Table 6.1; Item 4).

56 Complete the following procedure:

(1) Connect the signal generator as shown in Fig. 6.13.

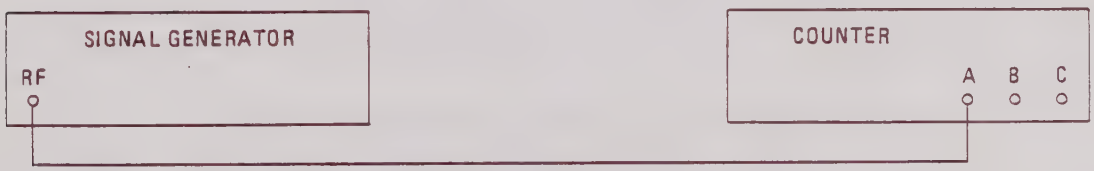


Fig. 6.13 Connections for Minimum Time Interval PVP

(2) Select 50 ohms on Input A, function TI A → B, and COM A.

(3) Select AUTO-TRIG, Ch. A and Ch. B slopes are the same.

(4) Set the signal generator output to 100 MHz at a level of 1V.

(5) Verify that a display of 0 ± 2 ns is obtained.

(6) Press the COM A key and ensure that its LED turns off.

(7) Disconnect the test equipment.

External Arming PVP

57 Required test equipment includes a signal generator and pulse generator (see Table 6.1; Items 4 and 6).

58 Complete the following procedure:

(1) Select 50 ohms on Input A and function FREQ A. Press the RESOLUTION ↓ key three times until 00000 is displayed.

(2) Connect the test equipment as shown in Fig. 6.14.

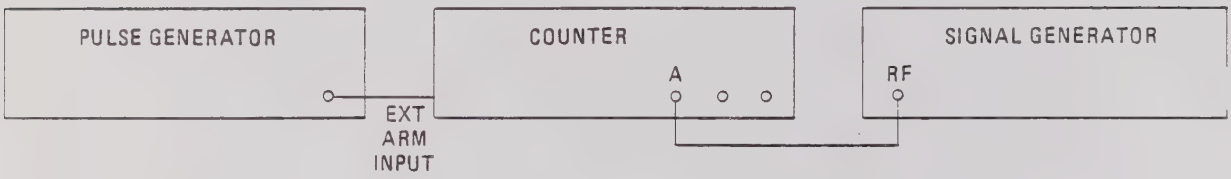


Fig. 6.14 Connections for External Arming PVP

(3) Set the signal generator output to 10 MHz at a level of 250 mV r.m.s.

(4) Prepare the pulse generator to provide a single, 300 μs, positive-going pulse with a low level of +0.8V and a high level of +2.8V (TTL-limit levels).

(5) Press the key sequence

[1] [6] [SHIFT] [STORE] [SF] [SHIFT] [SF] .

(6) Verify that the instrument is not counting.

(7) Trigger the pulse generator to obtain a single pulse output.

(8) Verify that the display indicates 10.0000 E 6 Hz ± 1 count and that the counter is not continuously gating.

(9) Press the key sequence

[1] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF] .

(10) Disconnect the test equipment.

Trigger Level PVP

59 Required test equipment includes an oscilloscope with probe and digital multimeter (see Figure 6.1; Items 2 and 3).

60 Complete the following procedure:

(1) Connect the test equipment as shown in Figure 6.15.

Fig. 6.15 Connections for Trigger Level PVP (I)

(2) Select the DC coupling of the oscilloscope input.

(3) Set the oscilloscope to monitor a waveform of approximately 12V peak-to-peak with a frequency of 2 Hz.

(4) Select the CHECK function.

(5) Press the key sequence

[7] [6] [SHIFT] [STORE] [SF] [SHIFT] [SF] .

(6) Verify that Input A and B TRIG LEDs are flashing, and that the displayed waveform is as shown in Fig. 6.16.

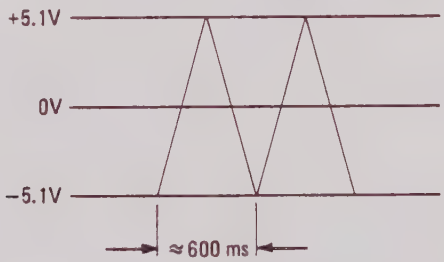


Fig. 6.16 Trigger Level Waveform

(7) Move the oscilloscope probe to the TRIGGER LEVEL B OUTPUT pin and verify that the same waveform is obtained.

(8) Press the key sequence

[7] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF] .

(9) Disconnect the test equipment.

61 Complete the following procedure:

(1) Connect the test equipment as shown in Figure 6.17.

Fig. 6.17 Connections for Trigger Level PVP (II)

(2) Set the multimeter to measure DC volts.

(3) For Inputs A and B, press the key sequence

TRIG LEVEL 5 TRIG LEVEL .

(4) Verify that the multimeter indicates +5V ± 60 mV.

(5) Move the oscilloscope probe to the TRIGGER LEVEL B OUTPUT pin and verify that the multimeter indicates +5V ± 60 mV.

(6) For Inputs A and B, press the key sequence

TRIG LEVEL 0 TRIG LEVEL .

(7) Verify that the multimeter indicates 0V ± 10 mV.

(8) Move the oscilloscope probe to the TRIGGER LEVEL A OUTPUT pin and verify that the multimeter indicates 0V ± 10 mV.

(9) Press the key sequence

TRIG LEVEL 5 SHIFT ± TRIG LEVEL .

(10) Verify that the multimeter indicates -5V ± 60 mV.

(11) Move the oscilloscope probe to the TRIGGER LEVEL B OUTPUT pin and verify that the multimeter indicates -5V ± 60 mV.

(12) Disconnect the test equipment.

Internal Frequency Standard PVP

62 Required test equipment includes a frequency standard (see Table 6.1; Item 1).

NOTE:

If either Option 04A or 04E ovenized frequency standard is installed, allow the counter to warm up for one hour (switched to standby, if required) before performing this procedure.

63 Complete the following procedure:

(1) Turn on the counter. Select function FREQ A. Verify that 00000000 is displayed. If Option 04E is installed, press the RESOLUTION key until 000000000 is displayed.

(2) Connect the test equipment as shown in Fig. 6.18.

Fig. 6.18 Connections for Internal Frequency Standard PVP

(3) Press key sequence

[1] [0] [EXP] [6] [SHIFT] [STORE] [X] .

(4) Press key sequence

[SHIFT] [RECALL] [X] .

Verify that 10.000000 6 is displayed.

(5) Press [CONTINUE] and key sequence [SHIFT] [R-X/Z] .

(6) Verify that the value displayed is within the limits shown in Table 6.8.

TABLE 6.8

Internal Frequency Standard Accuracy

Frequency Standard	Limits	
	Digits	Exp
Standard oscillator	±16	0
Option 04A	±3	0
Option 04E	±300	-3

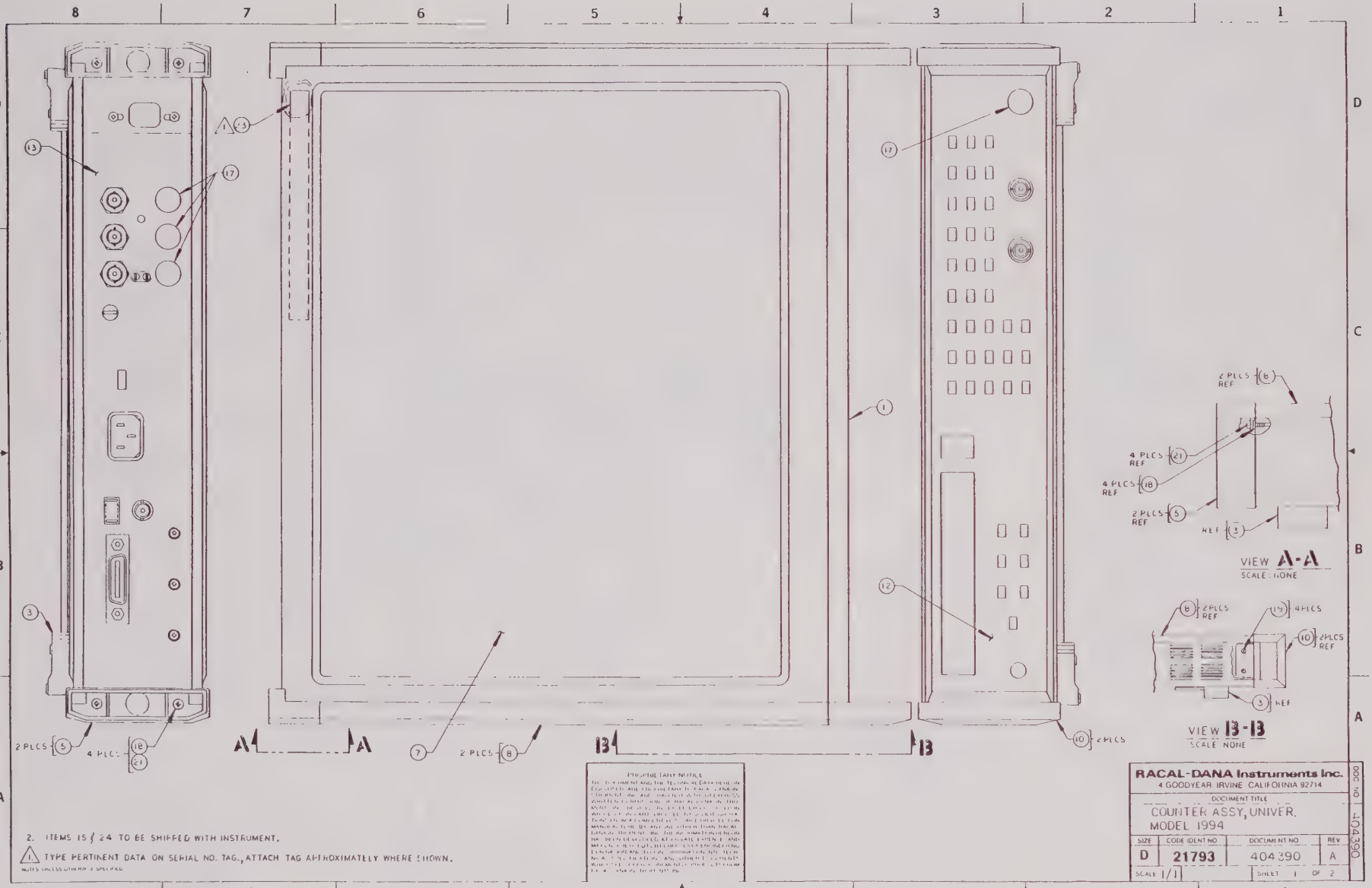
(7) Turn off the counter and disconnect the test equipment.

SECTION 7 DRAWINGS

404390	Counter Assembly	7-3
404391	Chassis Assembly	7-4
401730	PCB Assy., 10 MHz Oscillator	7-6
431730	Schematic, 10 MHz Oscillator	7-7
404426	PCB Assy., Motherboard	7-8
432159	Schematic, Motherboard	7-10
401746	PCB Assy., Display	7-14
431746	Schematic, Display	7-15
401760	PCB Assy., GPIB	7-17
431760	Schematic, GPIB	7-18
401762	PCB Assy., BNC	7-22
431762	Schematic, BNC	7-23

Options

404395	Option 01, Rear Input Assembly	7-24
404392	Option 04A, Oscillator Assembly	7-25
404397	Oven Oscillator	7-26
404384	Option 04E, Oscillator Assembly	7-27
404386	Oscillator	7-28
404691	Cable Assy., Oscillator	7-29
404399	Option 10, Reference Multiplier	7-30
19-1164	PCB Assy., Multiplier	7-31
432153	Schematic, Multiplier	7-32
404398	Option 41, Channel C	7-33
404389	PCB Assy., Channel C	7-34
432152	Schematic, Channel C	7-35



2. ITEMS 15 & 24 TO BE SHIPPED WITH INSTRUMENT.

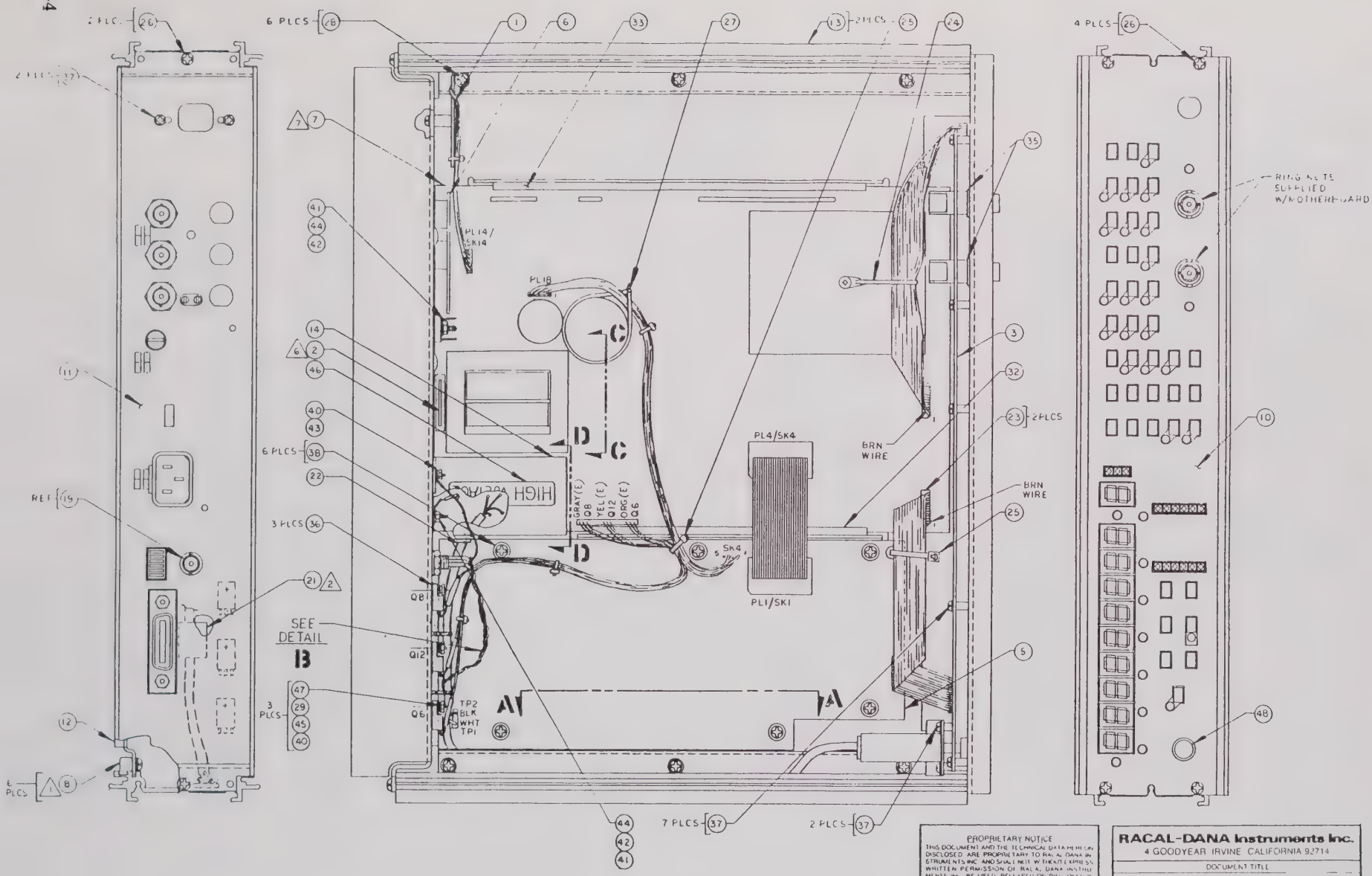
1. TYPE PERTINENT DATA ON SERIAL NO. TAG., ATTACH TAG APPROXIMATELY WHERE SHOWN.

NOTES UNLESS OTHERWISE SPECIFIED

PROPRIETARY NOTICE

RACAL-DANA Instruments Inc. 4 GOODYEAR IRVINE CALIFORNIA 92714			
DOCUMENT TITLE: COUNTER ASSY, UNIVER. MODEL 1994			
SIZE: D	CODE IDENT NO: 21793	DOCUMENT NO: 404390	REV: A
SCALE 1/1		SHEET 1 OF 2	

404390



NOTES: SEE SHEET 2

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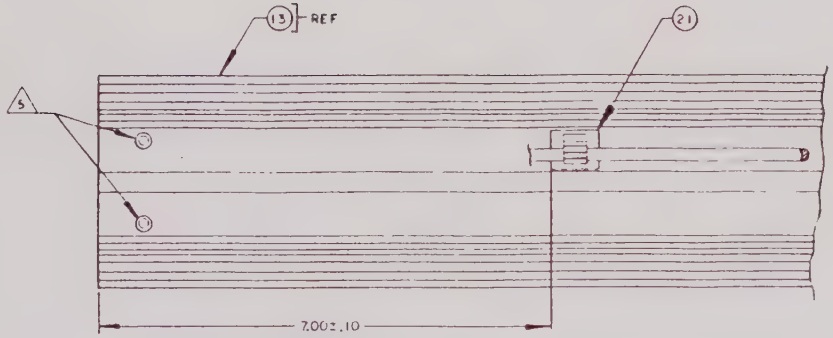
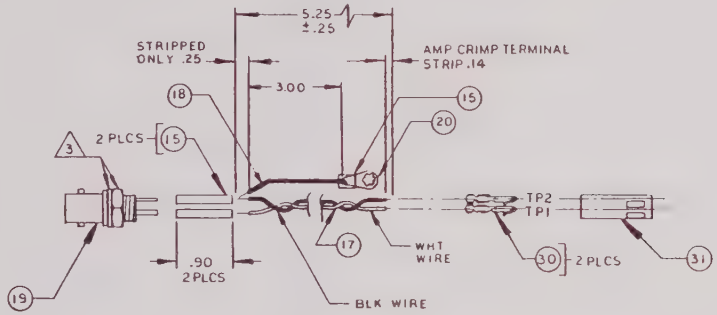
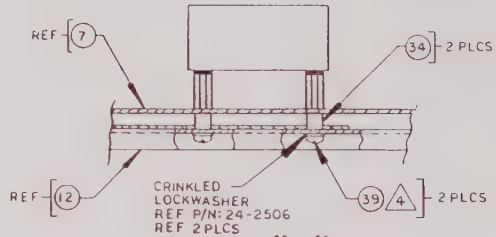
RACAL-DANA Instruments Inc.			
4 GOODYEAR IRVINE CALIFORNIA 92714			
DOCUMENT TITLE: CHASSIS ASSY			
SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	404391	E
SCALE 1/1		SHEET 1 OF 4	



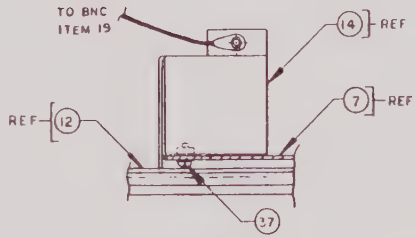
VIEW A-A
SCALE: NONE



DETAIL B
SCALE: NONE



SECTION C-C
SCALE: NONE



SECTION D-D
SCALE: NONE

7 LK4 (MOTHERBOARD) SHOULD BE JUMPERED BETWEEN PINS 1 & 2.

6 VOLTAGE SELECTION CARD, ITEM 2 SHOULD BE INSTALLED IN 120V POSITION

5 PEM NUTS TO BE AT FRONT PANEL END.

4 REMOVE EXISTING SCREW & CRINKLED LOCKWASHER & REPLACE WITH ITEM 34. USING CRINKLED LOCKWASHER (REF P/N 24-2506) PREVIOUSLY REMOVED. SECURE ITEM 34 TO BOTTOM SUPPORT PLATE WITH SCREW (ITEM 39).

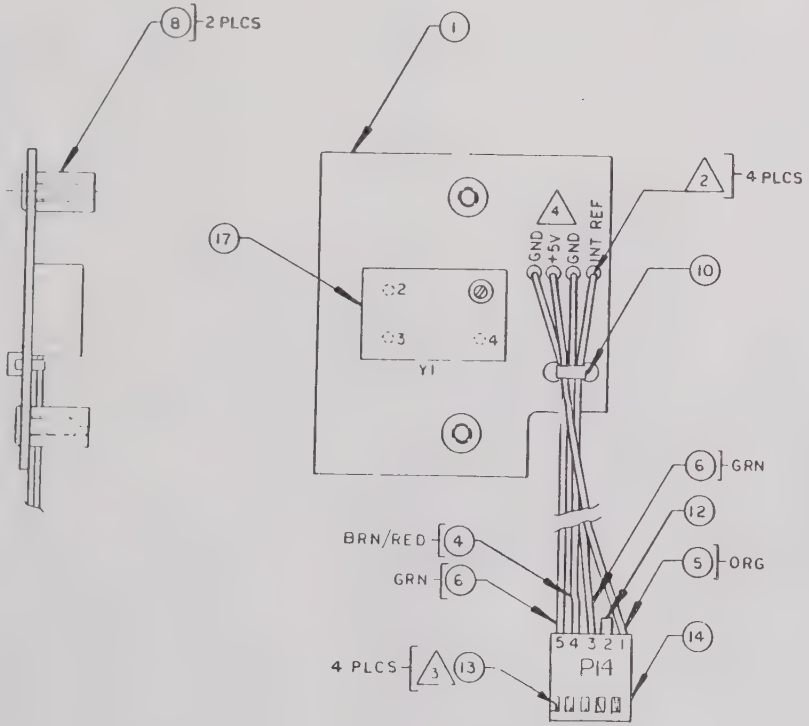
3 NUT & WASHER SUPPLIED WITH ITEM 19.

2 INSTALL ITEM 21 BETWEEN GPIB CONNECTOR AND TRANSISTORS ON INSIDE SURFACE OF REARPANEL.

1 INSTALL & ORIENT ITEM NO. 8 AS SHOWN.

NOTES UNLESS OTHERWISE SPECIFIED

SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	404391	E
SCALE —		SHEET 2 OF 4	



4 NOMENCLATURE SHOWN IS ON FARSIDE OF PC BOARD.

3 STRIP WIRE .14.

2 STRIP WIRE .25.

1. SCHEMATIC REF NO. 431730

NOTES UNLESS OTHERWISE SPECIFIED

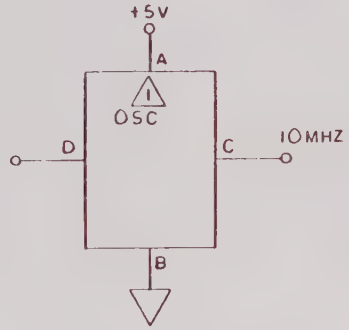
PROPRIETARY NOTICE

PCB ASSY, 10MHZ OSC.

SIZE	CODE IDENT NO	DRAWING NO	REV
C	21793	401730	A

SCALE 2:1 SHEET 1 OF 3

DOC NO 401730



OSC. VENDOR CHART

	P/N 921013 NDK	P/N 921014 TCXO	P/N 921013 SEI
A	4	2	2
B	2	4	1
C	3	1	3
D	1 (NC)	3 (NC)	4 (NC)

(1) FOR SPECIFIC PIN NUMBERS REFER TO OSC. VENDOR CHART.

NOTES UNLESS OTHERWISE SPECIFIED

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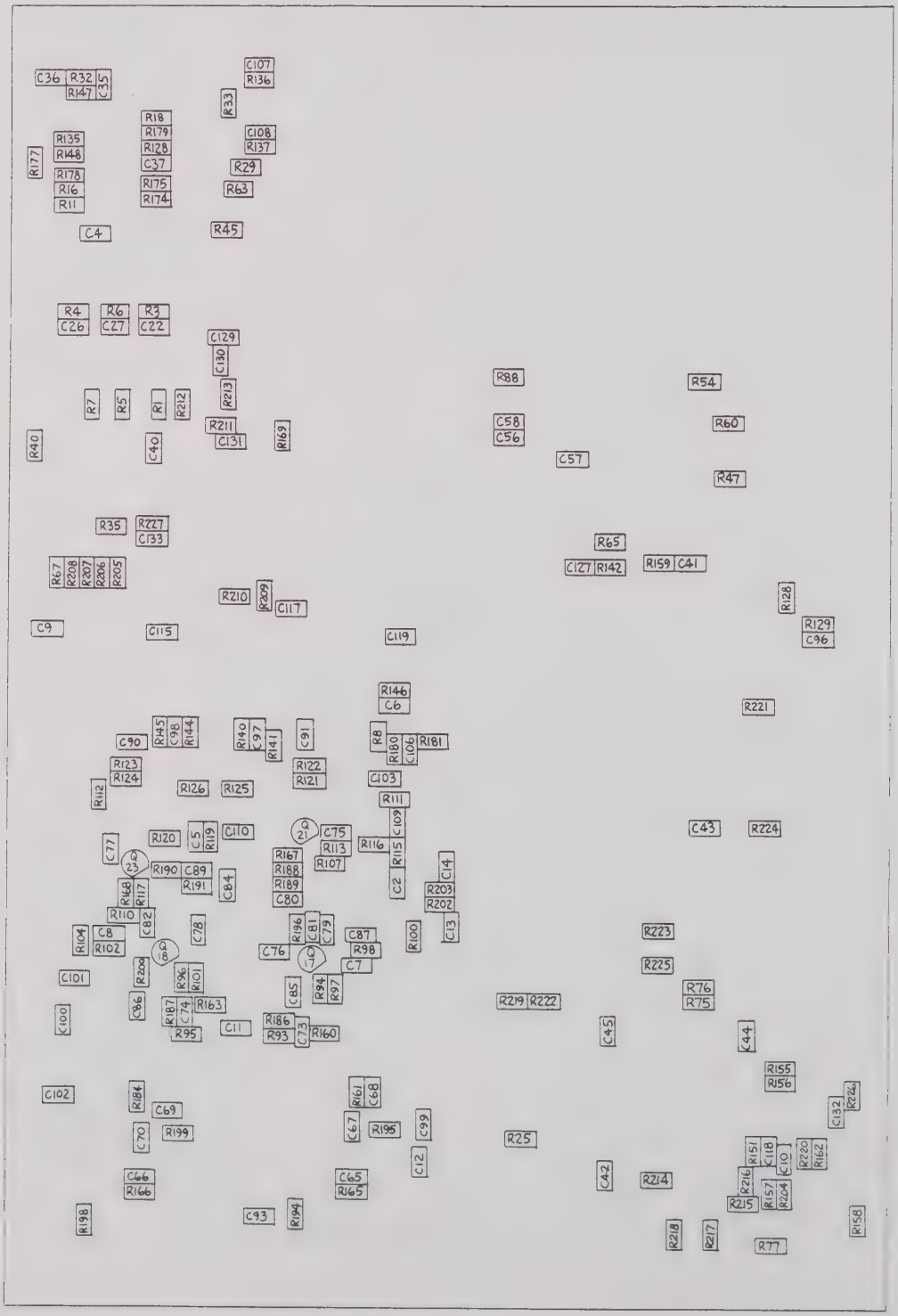
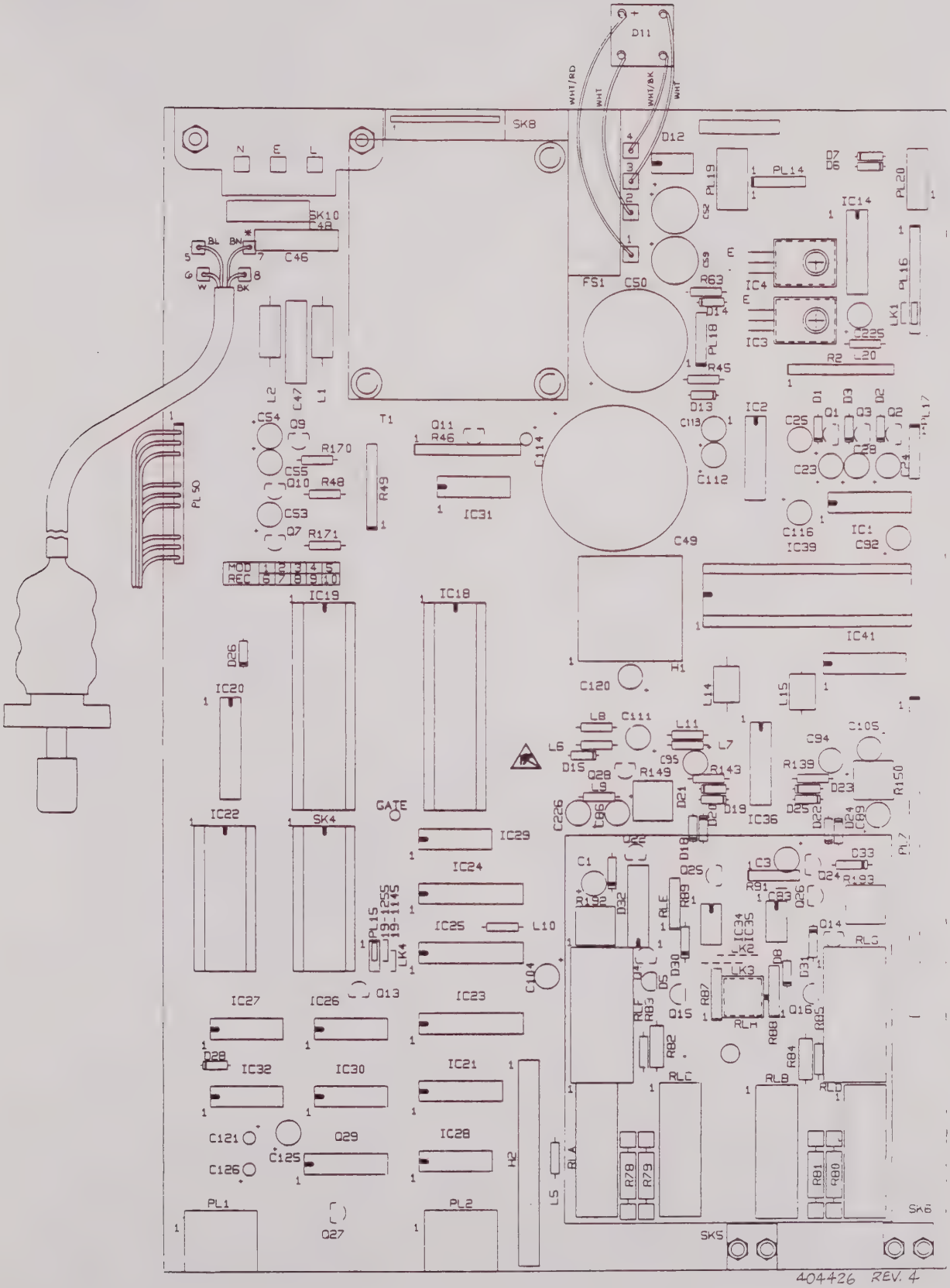
SCHEMATIC, 10MHZ OSC

SIZE	CODE IDENT NO	DWG NO	REV
B	21793	431730	A

SCALE —— SHEET 1 OF 1



CIRCUIT SIDE


D11
WHT/RD
WHT
WHT/BK
WHT
SK8
D12
PL19
PL14
D7
D6
PL20
IC14
SK10
C48
C46
BL
BN
BK
C52
C59
E
IC4
IC3
R63
D14
PL18
R45
FS1
C50
LK1
PL16
C225
R2
L20
L2
C47
L1
T1
C54
C58
R170
C55
Q10
R48
C53
Q7
R171
R49
Q11
R46
C114
IC31
D13
C113
C112
IC2
C26
Q1
Q3
Q2
D1
D3
D2
PL17
C28
C23
C24
C116
IC39
IC1
C92
C49
IC41
PL50
MOD
REC
IC19
IC18
D26
IC20
C120
H1
L14
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L8
C111
L11
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D15
C95
C94
C105
R139
R143
R149
Q28
D21
D23
R150
C226
D19
IC36
D25
D22
D24
C99
GATE
IC22
SK4
IC29
IC24
D18
D17
PL7
C1
D33
C3
Q25
R193
R91
Q24
R192
D32
Q26
D28
IC25
L10
PL15
19-1255
19-1145
LK4
C104
IC34
IC35
D14
RLG
LK2
LK3
D8
D31
IC27
IC26
Q13
IC23
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D5
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RLH
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Q16
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IC30
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C121
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C126
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IC28
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L5
RLA
R78
R79
R81
R80
PL1
Q27
PL2
SK6
SK5
404426 REV. 4

USED WITH SHT. 3

REF	PART No	TYP TYPE No.
D4 D6 D8	22 - 1029	1N4149
Q11	22 - 4216	CA3085
IC29	22 - 4535	74LS02
IC26	22 - 4551	74LS11
IC28	22 - 4557	74LS10
IC4	22 - 4562	MC1025
IC21	22 - 4576	74LS32
IC22	22 - 4585	74LS393
IC5	22 - 4567	74LS138
IC35	22 - 6100	CD4011
IC32	22 - 4156	6C106
IC23	22 - 4007	74HCT244
IC2025	22 - 4008	74HCT373
Q5	22 - 6007	2N3904
Q4	22 - 6008	2N3906
Q12	22 - 6113	ZTX550
IC19	22 - 8301	146854E
IC18	22 - 8403	MC1
IC39	22 - 8404	MC2
IC22	22 - 6578	81LS6

USED WITH SHT. 4

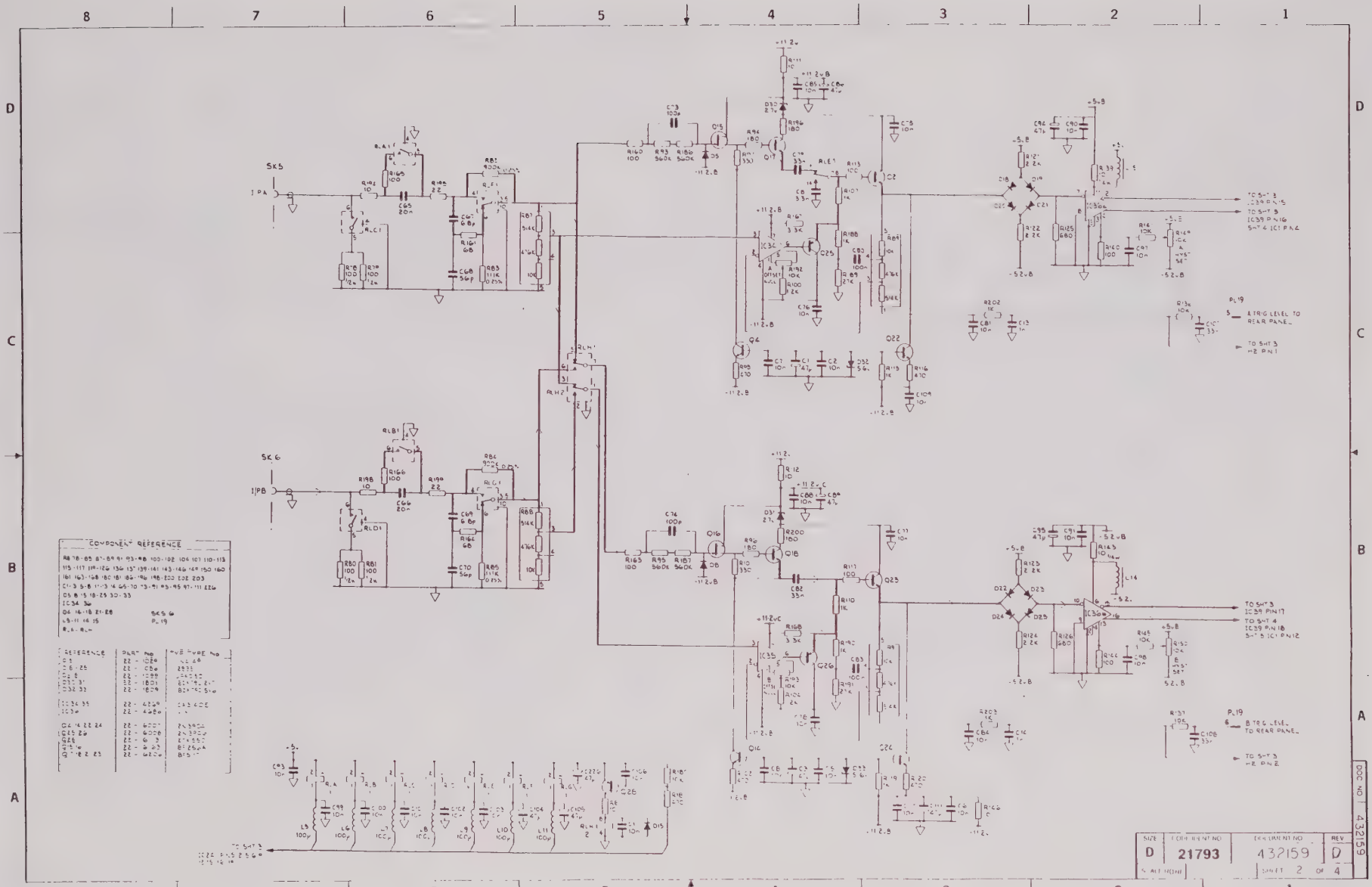
REF	PART No	TYP TYPE No.
D13 67 13,14	22 - 1029	1N4149
D11	22 - 1662	VH248
D12	22 - 1666	B40C800
IC3	22 - 4219	7812CT
IC31	22 - 4262	MC3403
IC4	22 - 4294	7912CT
IC2 14	22 - 4528	10116
IC1	22 - 4590	10216

REF	PART No	TYP TYPE No.
Q11	22 - 6007	2N3904
Q1-3	22 - 6018	MPS3640
Q9 10	22 - 6112	ZTX450
Q7	22 - 6113	ZTX550
Q6	22 - 6152	BDT91
Q8,12	22 - 6153	BDT92

COMPONENT REFERENCE		
R1-7, 11, 16, 18, 32 35, 40 45-49, 54, 60, 63, 68, 135, 147, 148, 159, 170, 171, 174, 175, 177-179, 211-213, 226		
C4, 22-28, 35-37, 40, 41, 46-50, 52-59, 112-114, 128-132, 225		
D1-3, 67, 11-14.	FS1	
IC1-4, 14, 31	B1	LK1
Q1-3 6-12	T1	
L1, 2 20	SK8 10	
	P-2, 14, 16, 17 20, 21	

RACAL-DANA Instruments Inc. 4 GODDYEAR IRVINE CALIFORNIA 92714				
SCHEM MOTHERBOARD				
SIZE D	CODE IDENT NO 21793			REV D
			SHEET 1 OF 4	

DO NOT SCALE 43259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SK6
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RLB1
RLC1
RLD1
RLE1
RLG1
RLH1
RLH2
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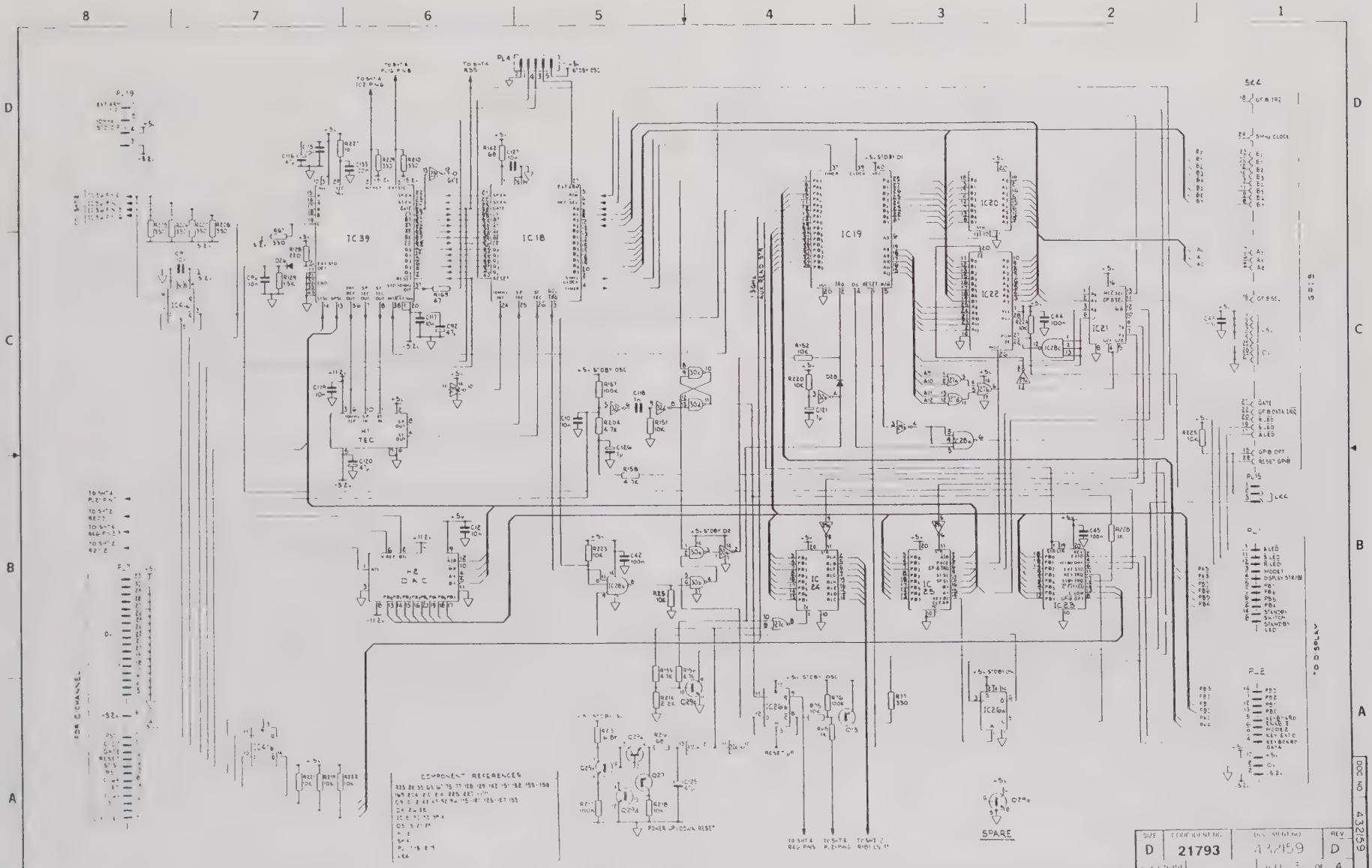
C40


IC39
IC18
IC19
IC20
IC22
IC21
IC24
IC25
IC23
IC26
IC28
TEC
DAC
SPARE
COMPONENT REFERENCES
SIZE
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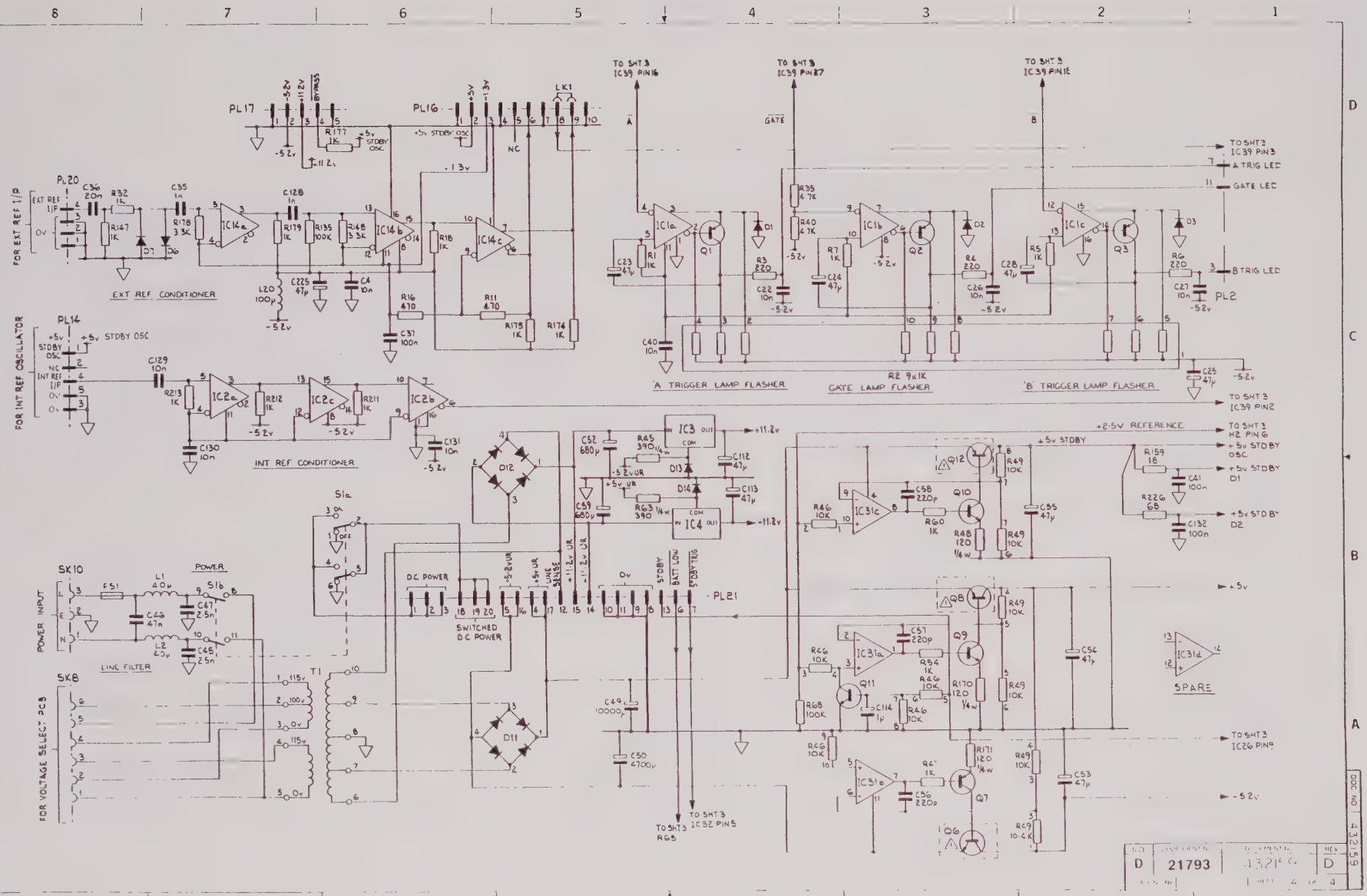
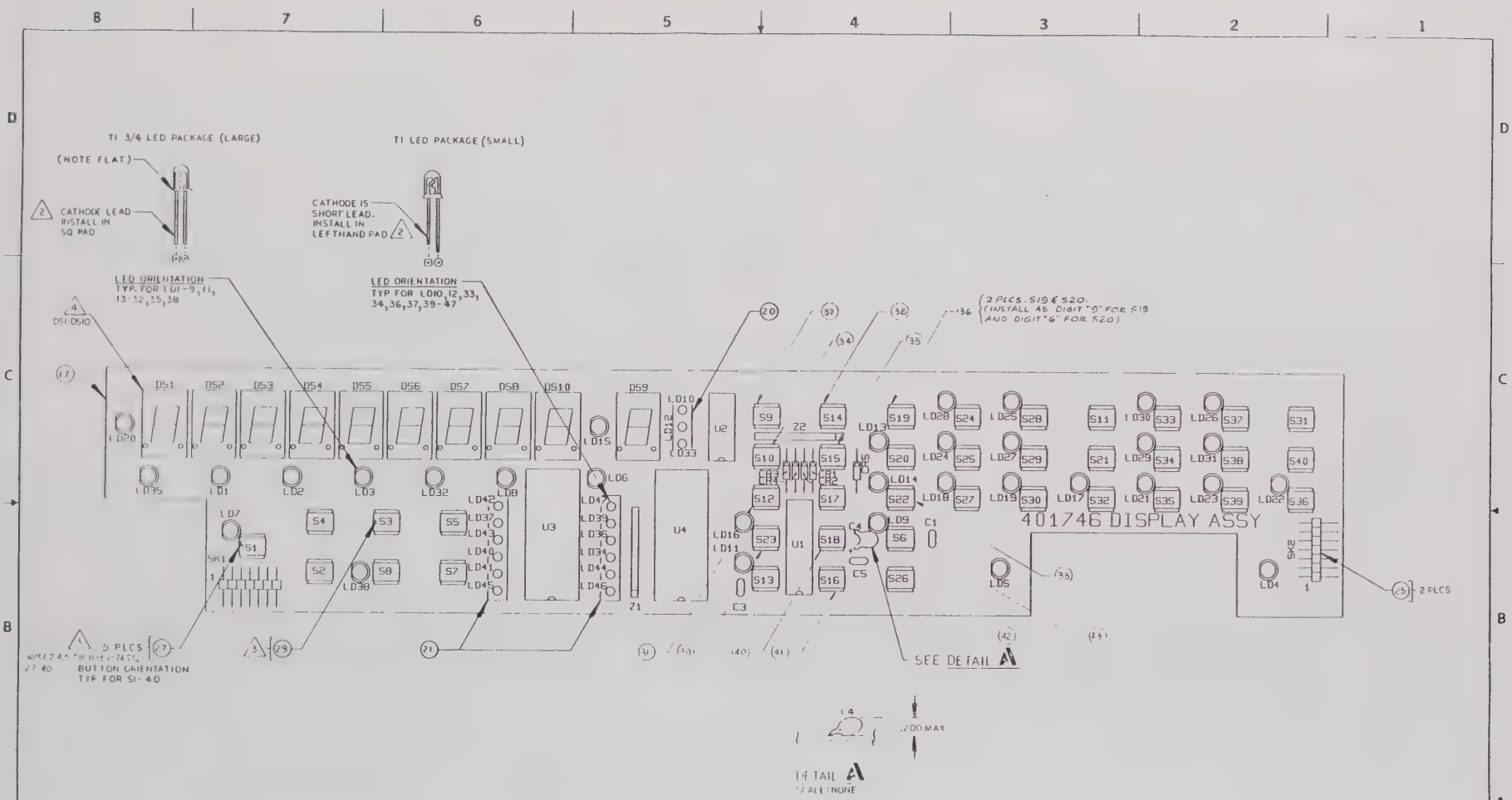
CODE IDENT NO.
21793
DWG NO.
42159
REV
D
SHEET 3 OF 4


PL17
PL16
PL20
PL14
PL2
PL21
LK1
BYPASS
EXT REF CONDITIONER
INT REF CONDITIONER
FOR EXT REF I/P
FOR INT REF OSCILLATOR
A TRIGGER LAMP FLASHER
GATE LAMP FLASHER
'B' TRIGGER LAMP FLASHER
R2 9x1K
+2·5V REFERENCE
SPARE
POWER
POWER INPUT
LINE FILTER
FOR VOLTAGE SELECT PCB
SWITCHED D.C POWER
D.C POWER
TO SHT 3 IC39 PIN16
TO SHT 3 IC39 PIN17
TO SHT 3 IC39 PIN18
TO SHT 3 IC39 PIN3
A TRIG LED
GATE LED
B TRIG LED
TO SHT 3 IC39 PIN2
TO SHT 3 H2 PIN6
TO SHT 3 IC26 PIN9
TO SHT 3 IC32 PIN5
TO SHT 3 RG5
+5v STDBY OSC
+5v STDBY D1
+5v STDBY D2
+5v STDBY
GATE
NC
D
21793
DOC NO 4321/59


TI 3/4 LED PACKAGE (LARGE)
(NOTE FLAT)
CATHODE LEAD INSTALL IN SQ PAD
TI LED PACKAGE (SMALL)
CATHODE IS SHORT LEAD. INSTALL IN LEFTHAND PAD
LED ORIENTATION TYP. FOR LD1-9,11, 13-32,35,38
LED ORIENTATION TYP FOR LD10,12,33, 34,36,37,39-47
DS1-DS10
2 PLCS. S19 & S20. (INSTALL AS DIGIT "9" FOR S19 AND DIGIT "6" FOR S20)
401746 DISPLAY ASSY
2 PLCS
5 PLCS
BUTTON ORIENTATION TYP FOR S1-40
SEE DETAIL A
.200 MAX
DETAIL A
SCALE:NONE

4 DS1-DS10 TO BE INSTALLED USING THE SAME INTENSITY CODE.

3 ENSURE BUTTON IS FIRMLY SEATED ON SWITCH.

2 INSTALL ALL LEDS (LD1-LD47) AND SWITCHES (S1-S40) FLUSH TO PCB.

1 REFERENCE SCHEMATIC 401746

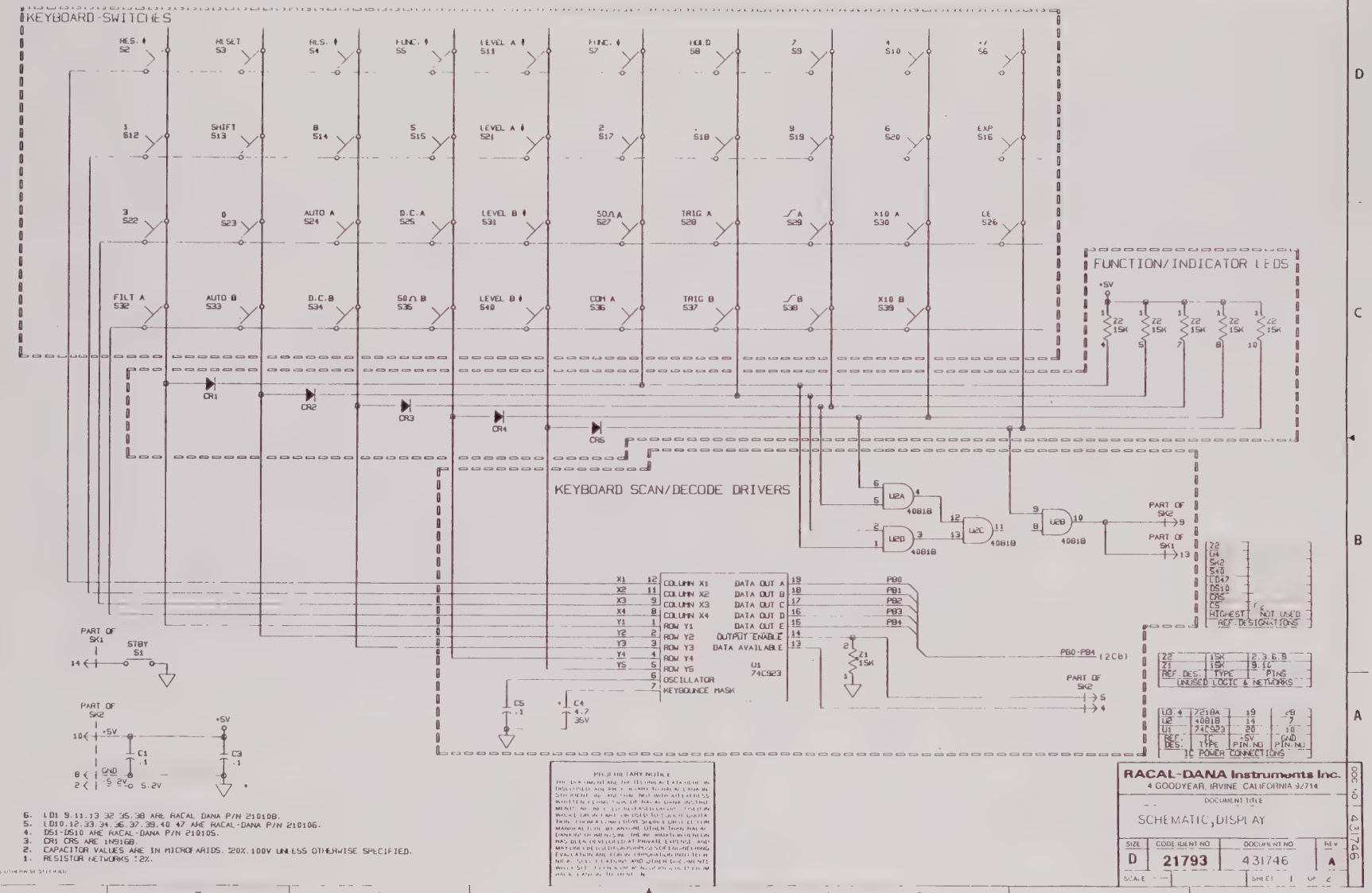
RACAL-DANA Instruments Inc.
4 GOODYEAR IRVINE CALIFORNIA 92714

DOCUMENT TITLE
PCB ASSY, DISPLAY

SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	401746	C

SCALE 2/1 SHEET 1 OF 3

DOC NO 401746



6. LD1 9.11.13 32 35.38 ARE RACAL DANA P/N 210108.
5. LD10.12.33.34.36.37.39.40 47 ARE RACAL-DANA P/N 210106.
4. DS1-DS10 ARE RACAL-DANA P/N 210105.
3. CR1 CR5 ARE 1N9168.
2. CAPACITOR VALUES ARE IN MICROFARIDS. 20%. 100V UNLESS OTHERWISE SPECIFIED.
1. RESISTOR NETWORKS ±2%.

NOTES UNLESS OTHERWISE STATED:

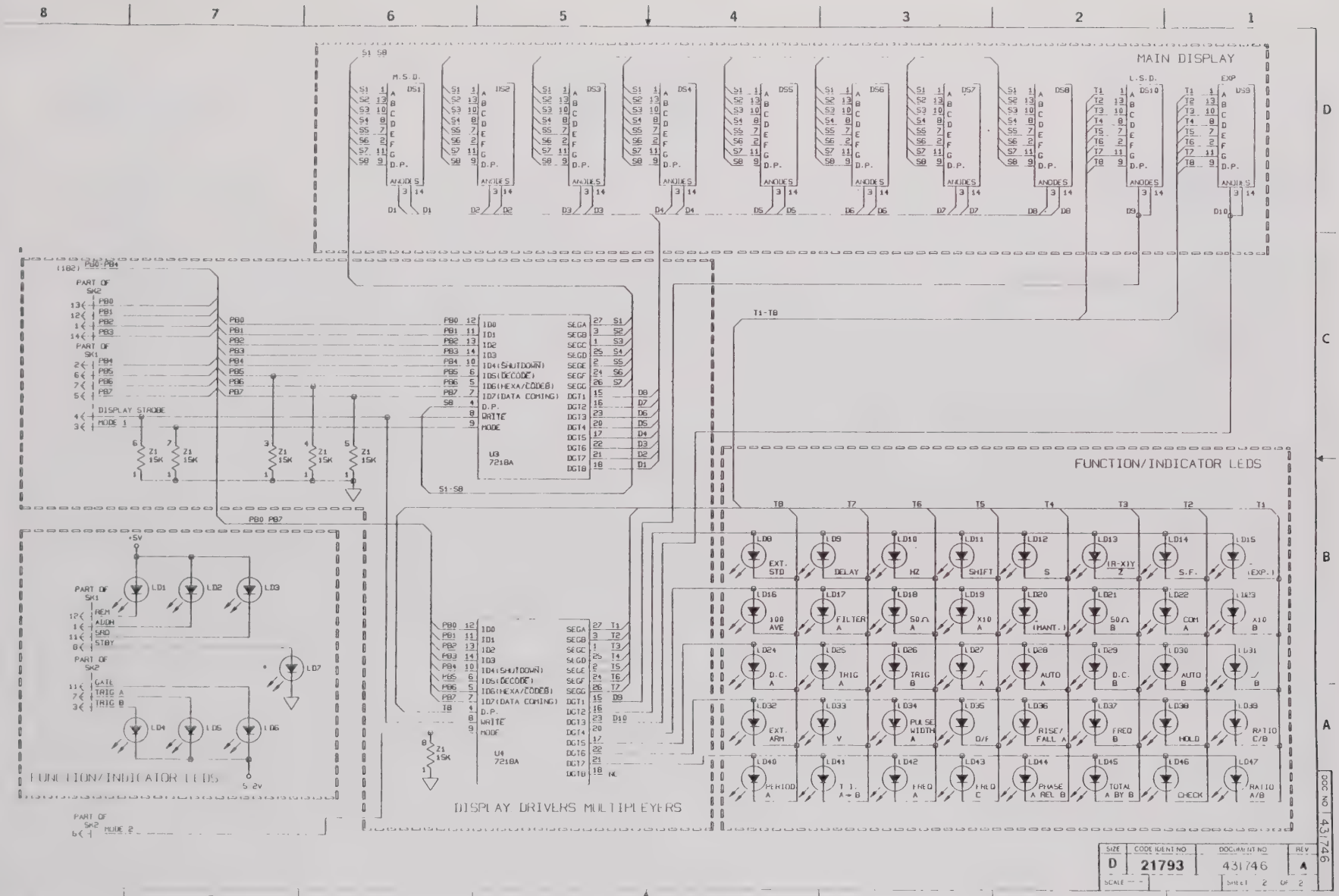
RACAL-DANA Instruments Inc.
4 GOODYEAR, IRVINE CALIFORNIA 92714

DOCUMENT TITLE
SCHEMATIC, DISPLAY

SIZE	CODE IDENT NO.	DOCUMENT NO.	REV
D	21793	431746	A

SCALE — SHEET 1 OF 2

DOC NO 431746



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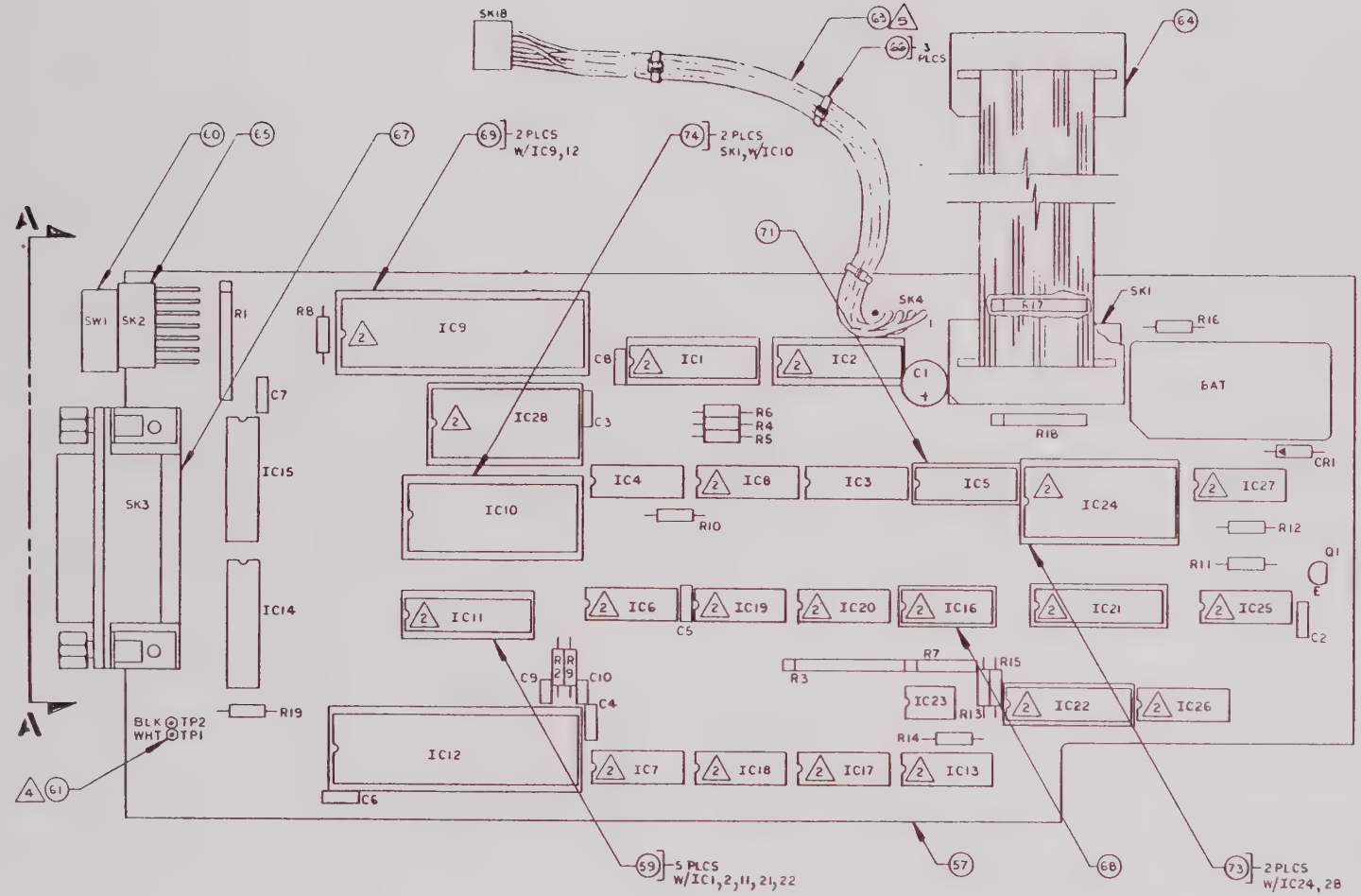
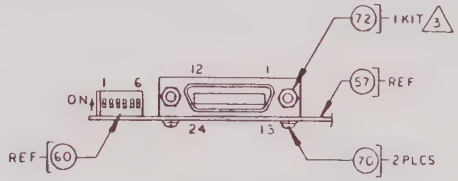
D	21793	431746	A
SCALE —		SHEET 2 OF 2	

DOC NO 431746





VIEW A - A
SCALE: NONE

5 TO WIRE ITEM 63 USE SHEET No. 5.

4 INSTALL WITH SHORT LEADS IN PCB.

3 DISCARD NUTS (2) & LOCKWASHERS (2) SUPPLIED WITH ITEM 72.

2 IC1, 2, 6-9, 11, 13, 16-22, & 24-28 ARE STATIC SENSITIVE DEVICES.

1. REFERENCE SCHEMATIC 431760.

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RACAL-DANA Instruments Inc.			
4 GOODYEAR, IRVINE CALIFORNIA 92714			
DOCUMENT TITLE			
PCB ASSY, GPIB			
SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	401760	D
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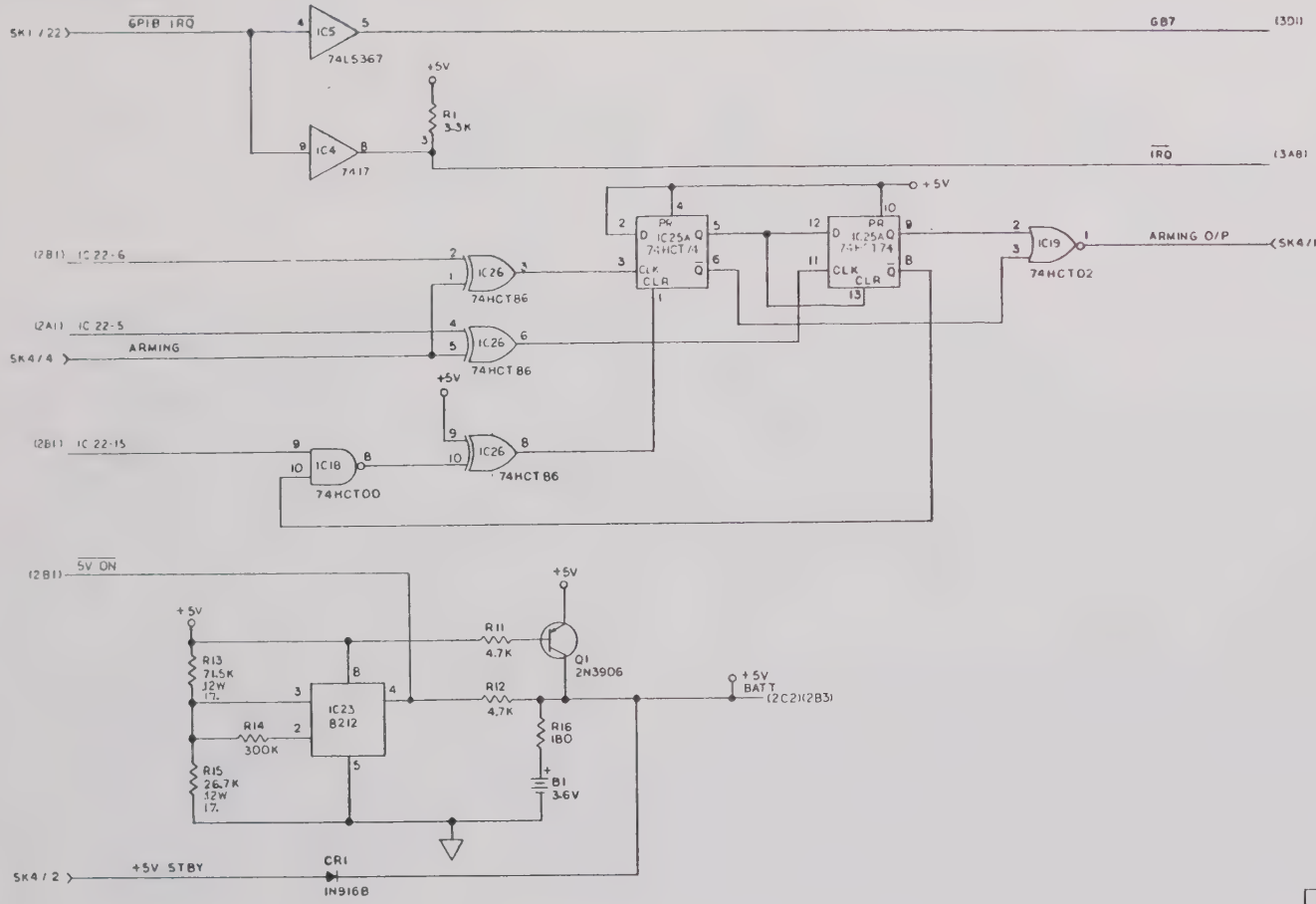

TP2	
SW1	
SK4	
R19	
Q1	
IC28	
CR1	
C10	
HIGHEST	NOT USED

REFERENCE DESIGNATIONS

REF. DES.	IC TYPE	V+ PIN NO	GND PIN NO
IC 26	74HCT86	14	7
IC 24,28	8417 2	24	12
IC 23	8212	8	5
IC20,27	74HCT32	14	7
IC16,17,25	74HCT74	14	7
IC15	75160	20,11	10
IC14	75161	20,11	10
IC13	4066A	14	7
IC12	6848B	20	1,2
IC11	74HCT373	20	1,10
IC10	27128	1,28	14
IC9	6805E3	——	20
IC8	74HCT138	16	8
IC7,18	74HCT00	14	7
IC6,19	74HCT02	14	7
IC5	74LS367	16	8
IC4	7417	14	7
IC3	74F138	16	8
IC1,2,21,22	74HCT374	20	10

IC POWER CONNECTIONS

4 RESISTOR NETWORKS ARE PULLED UP TO +5V VIA PIN1 OF EACH NETWORK.

3 RESISTOR NETWORKS ARE 1/1W 2%.
RESISTORS R17 AND R18 VALUES ARE 100K R7 1% 9W

2 RESISTOR VALUES ARE IN OHMS, 1/4W 5%.

1 CAPACITOR VALUES ARE IN UF, 100V, 20%.

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DOCUMENT TITLE
SCHEMATIC
G.P.I.B

SIZE	CODE IDENT NO	DOCUMENT NO	REV
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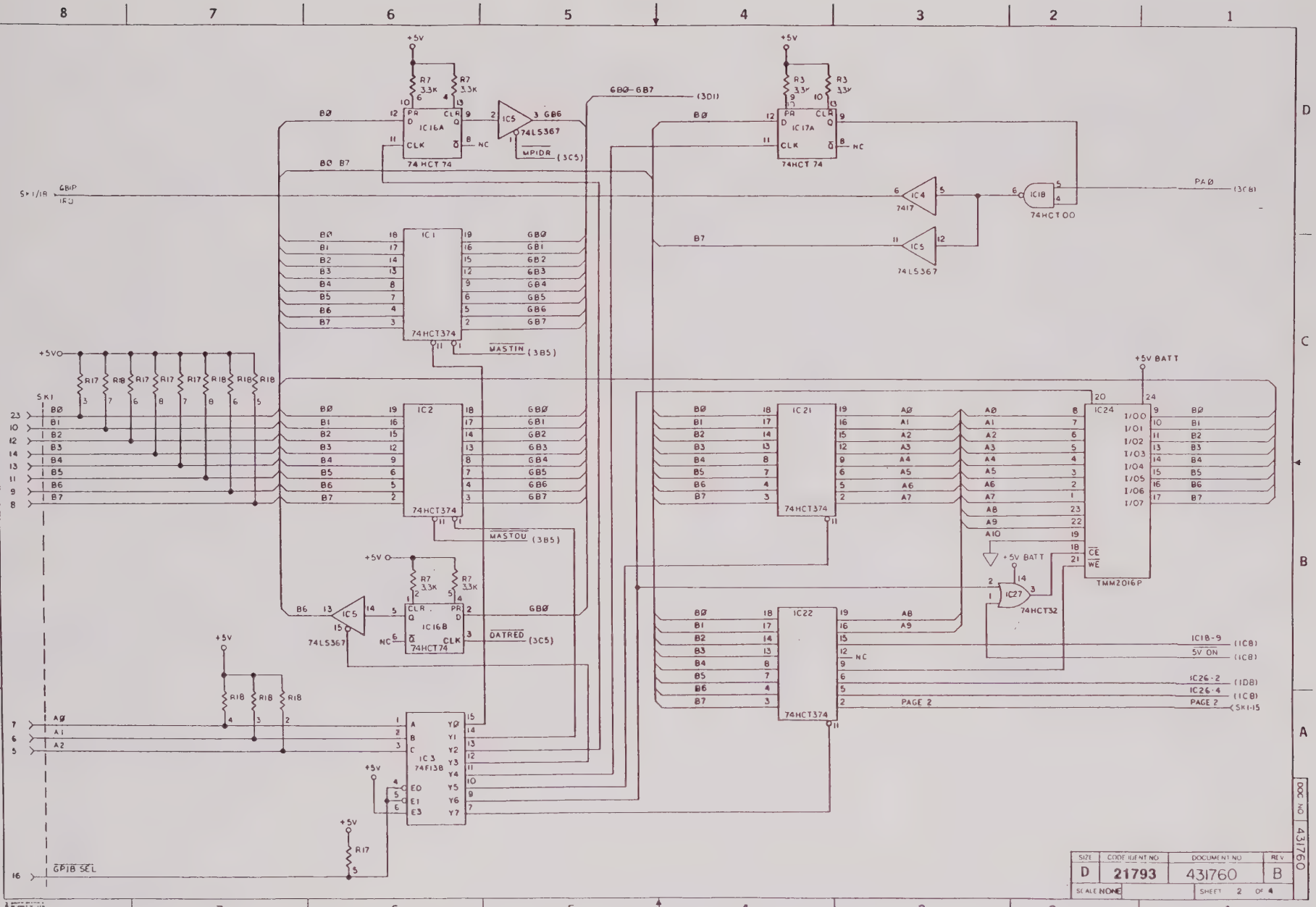
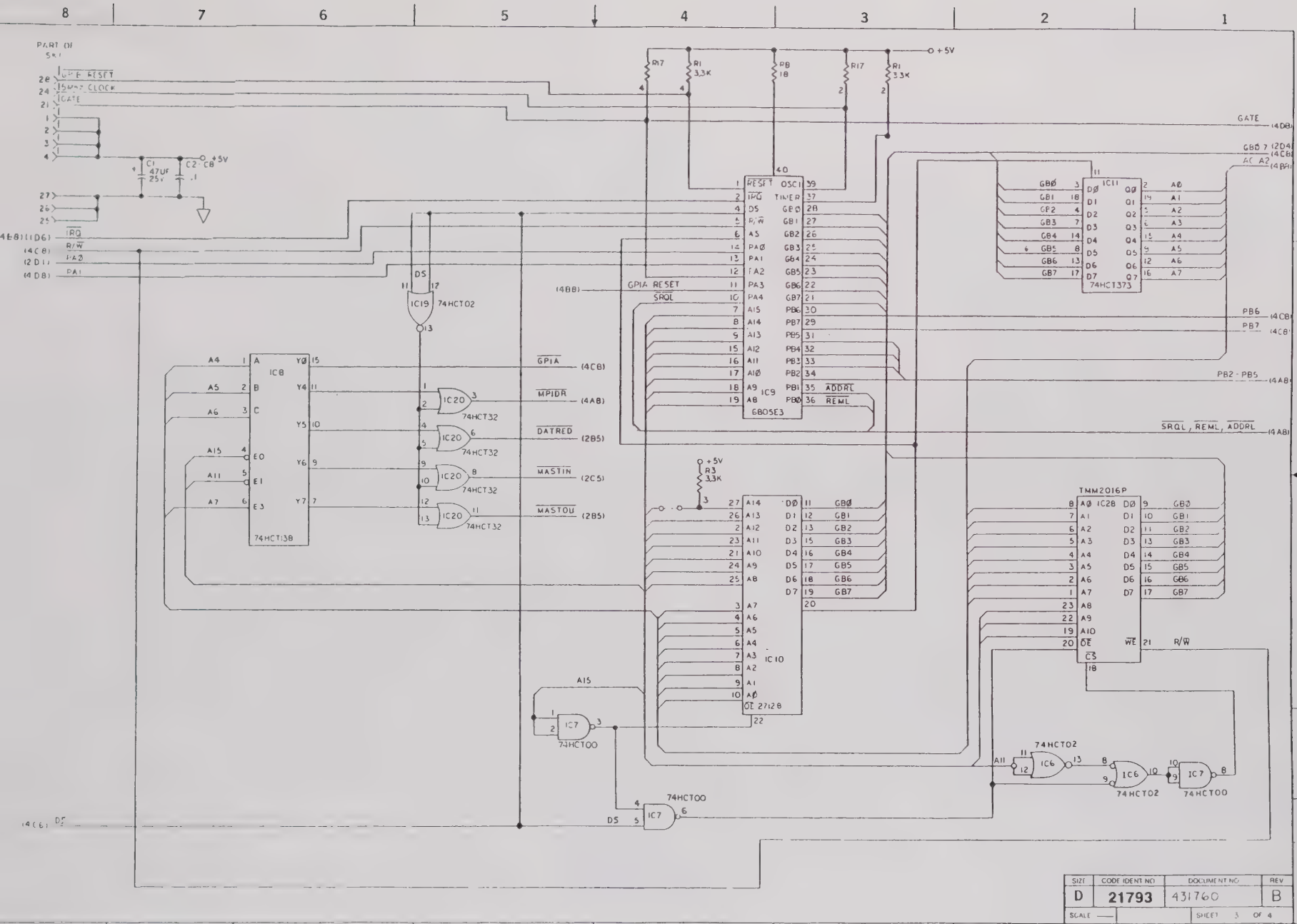
SCALE NONE | SHEET 1 OF 4

DOC NO 431760


+5V
R7 3.3K
IC16A
74HCT74
74LS367
IC5
GB0-GB7
(3D1)
MPIDR
(3C5)
B0 B7
GBIP IRQ
IC17A
IC4
7417
IC18
74HCT00
PA0
(3C6)
IC1
74HCT374
MASTIN
(3B5)
+5VO
R17
R18
SK1
IC2
MASTOU
(3B5)
+5V BATT
IC21
IC24
TMM2016P
IC16B
DATRED
(3C5)
IC27
74HCT32
IC22
IC18-9
(1C8)
5V ON
(1C8)
IC26-2
(1D8)
IC26-4
(1C8)
PAGE 2
SK1-15
IC3
74F138
GPIB SEL
SIZE
D
CODE IDENT NO
21793
DOCUMENT NO
431760
REV
B
SCALE NONE
SHEET 2 OF 4
DOC NO 431760



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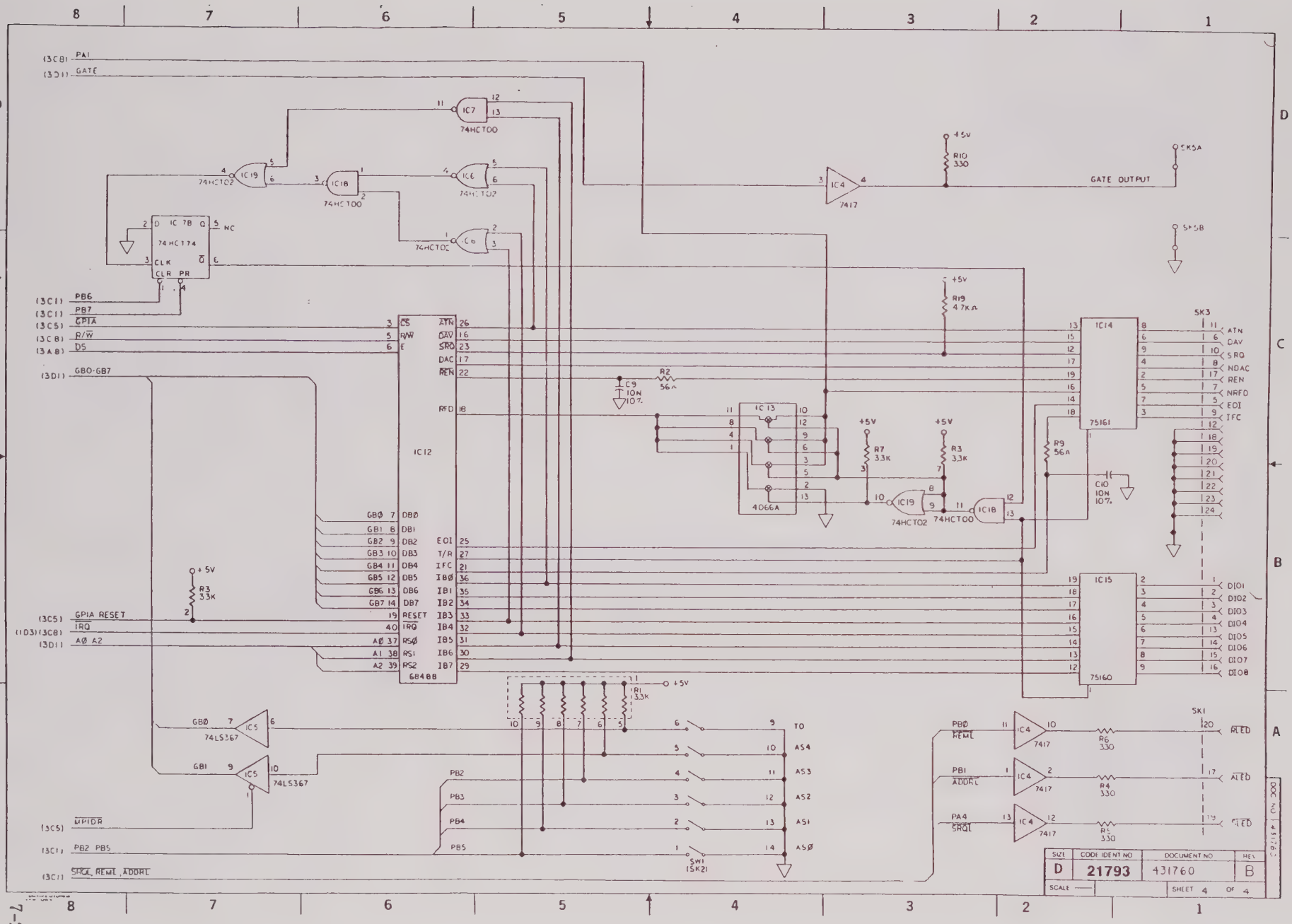
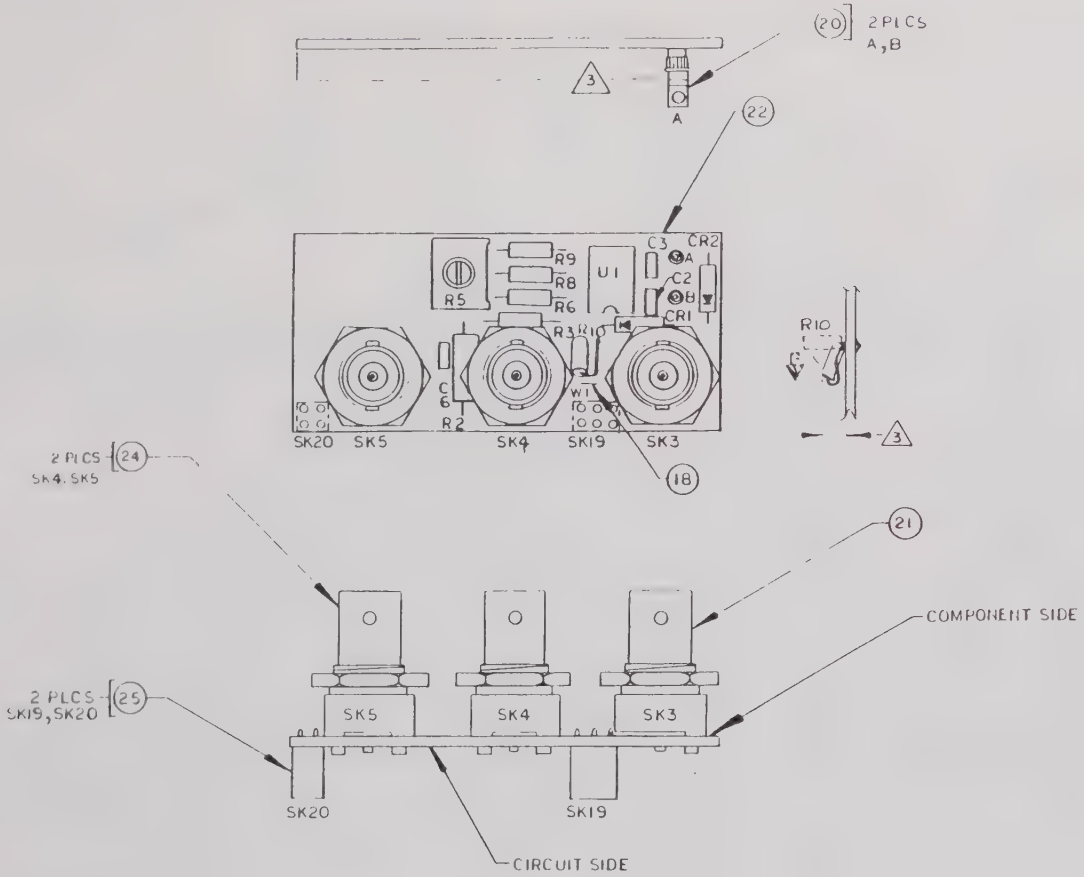
SCALE —		SHEET 3 OF 4	


(3C8) PA1
(3D1) GATE
IC7 74HCT00
IC19 74HCT02
IC18 74HCT00
IC6 74HCT02
IC6 74HCT02
IC 7B 74HC174
NC
CLR PR
(3C1) PB6
(3C1) PB7
(3C5) GPIA
(3C8) R/W
(3A8) DS
(3D1) GB0-GB7
IC12
CS
R/W
E
ATN 26
DAV 16
SRQ 23
DAC 17
REN 22
RFD 18
GB0 7 DB0
GB1 8 DB1
GB2 9 DB2
GB3 10 DB3
GB4 11 DB4
GB5 12 DB5
GB6 13 DB6
GB7 14 DB7
EOI 25
T/R 27
IFC 21
IB0 36
IB1 35
IB2 34
IB3 33
IB4 32
IB5 31
IB6 30
IB7 29
RESET 19
IRQ 40
A0 37 RS0
A1 38 RS1
A2 39 RS2
68488
(3C5) GPIA RESET
(1D3)(3C8) IRQ
(3D1) A0 A2
+5V
R3 3.3K
IC4 7417
R10 330
GATE OUTPUT
SK5A
SK5B
R19 4.7KΩ
C9 10N 10%
R2 56Ω
IC13 4066A
R7 3.3K
R3 3.3K
IC19 74HCT02
IC18 74HCT00
R9 56Ω
C10 10N 10%
IC14 75161
IC15 75160
SK3
ATN
DAV
SRQ
NDAC
REN
NRFD
EOI
IFC
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
R1 3.3K
IC5 74LS367
GB0
GB1
(3C5) GPIDR
(3C1) PB2 PB5
(3C1) SRQL REML ADDRL
PB2
PB3
PB4
PB5
TO
AS4
AS3
AS2
AS1
AS0
SW1 (SK2)
PB0 REML
PB1 ADDRL
PA4 SRQL
R6 330
R4 330
R5 330
SK1
REN
ATN
EOI
SIZE D
CODE IDENT NO 21793
DOCUMENT NO 431760
REV B
SCALE
SHEET 4 OF 4



3 .250 MAX. HEIGHT FOR ALL COMPONENTS EXCEPT FOR ITEMS 20, 24 & 25.

2. CR1, CR2, & R3, R6, R8, R9 TO BE INSTALLED ON .45 CENTERS.

1. REFERENCE SCHEMATIC 431702.

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DOCUMENT TITLE
PCb ASSY, BNC

SIZE	CODE IDENT NO	DOCUMENT NO	REV
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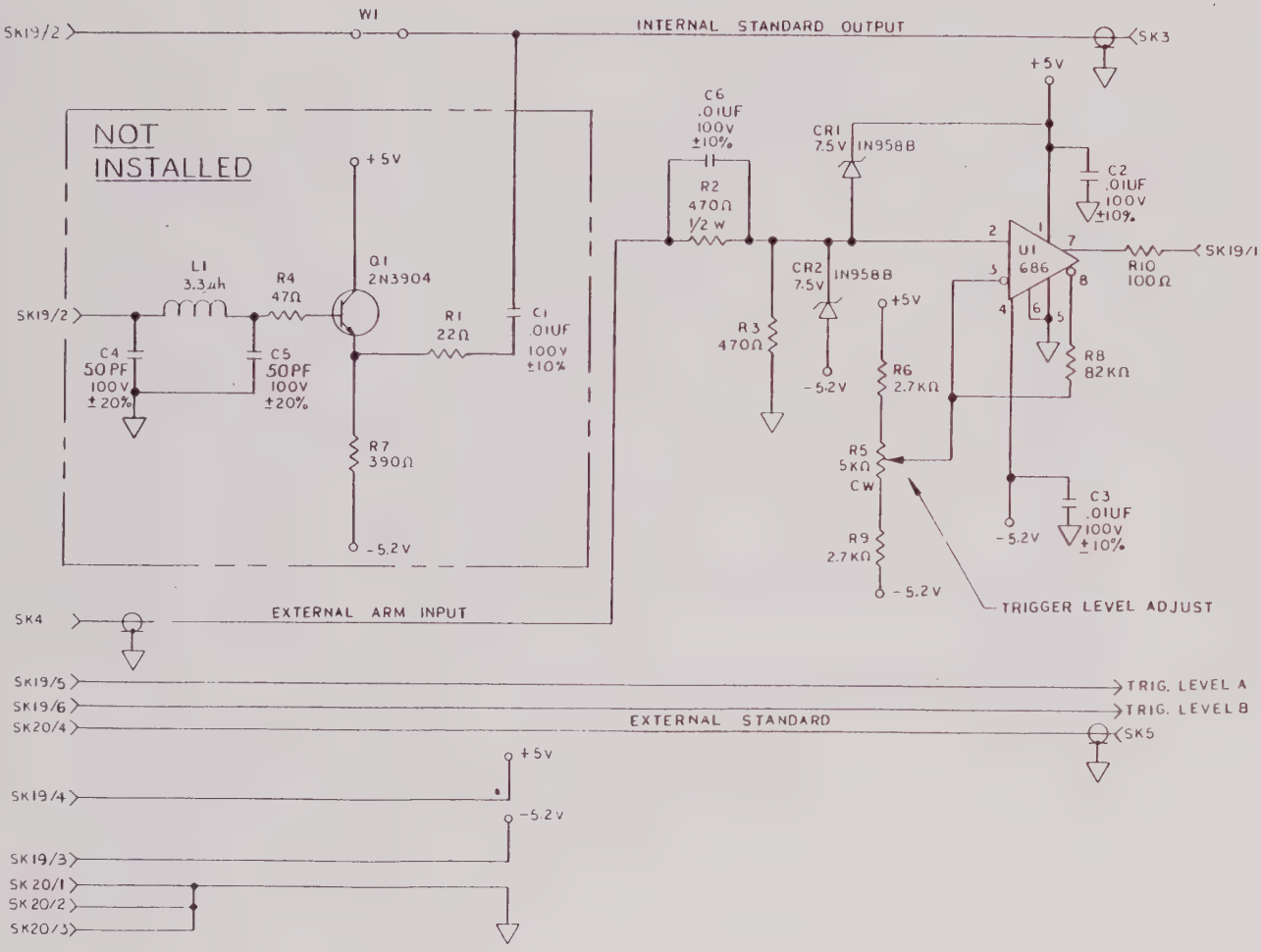
SCALE 2:1 SHEET 1 OF 2

SEE DWG 401762



1. RESISTOR VALUES ARE 1/4 WATT, ± 5%.

NOTES UNLESS OTHERWISE SPECIFIED

L1	
B	
U1	
SK20	
R10	
Q1	
CR2	
C6	
HIGHEST	NOT USED

REFERENCE DESIGNATIONS

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DOCUMENT TITLE

SCHEM, BNC

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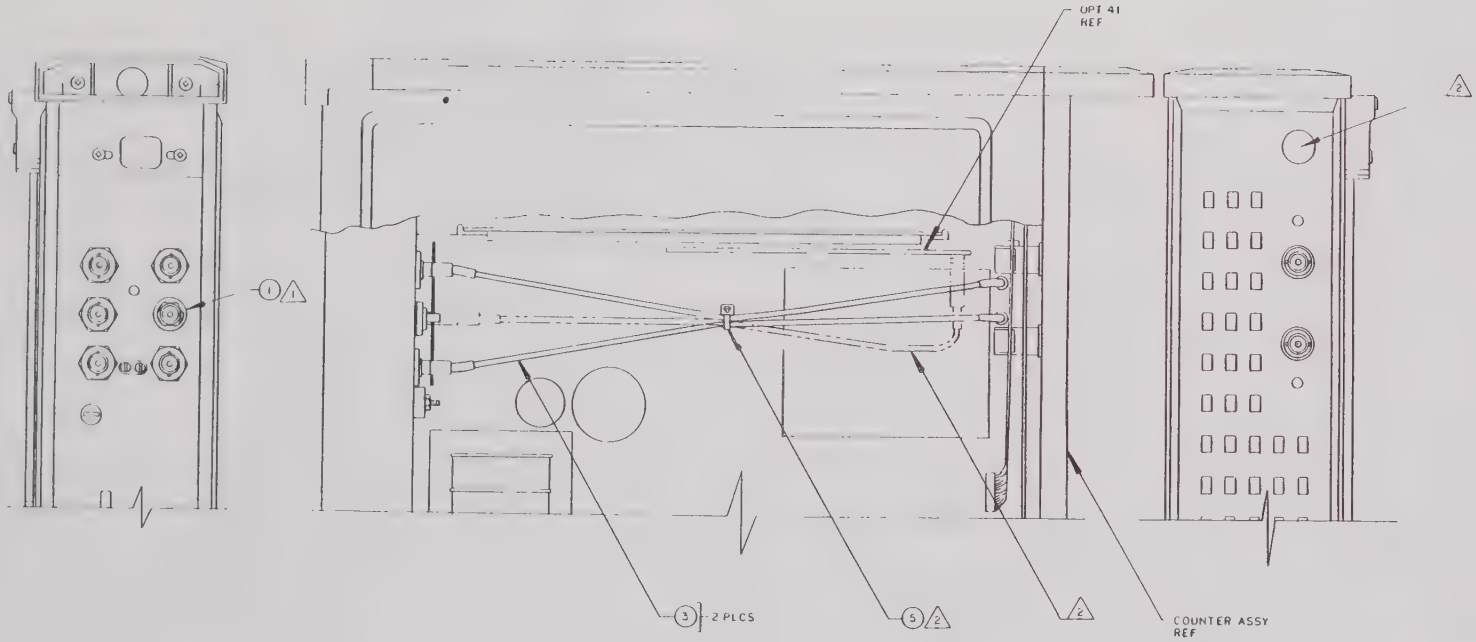

2 IF OPTION 41 IS INSTALLED, UNPLUG CABLE FROM FRONT BNC AND PLUG TO ITEM 1.

1 LOCKNUT SUPPLIED WITH BNC ITEM 1.

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DOCUMENT TITLE
REAR INPUT ASSY, A6B
OPTION 01

SIZE	CODE IDENT NO	DOCUMENT NO	REV
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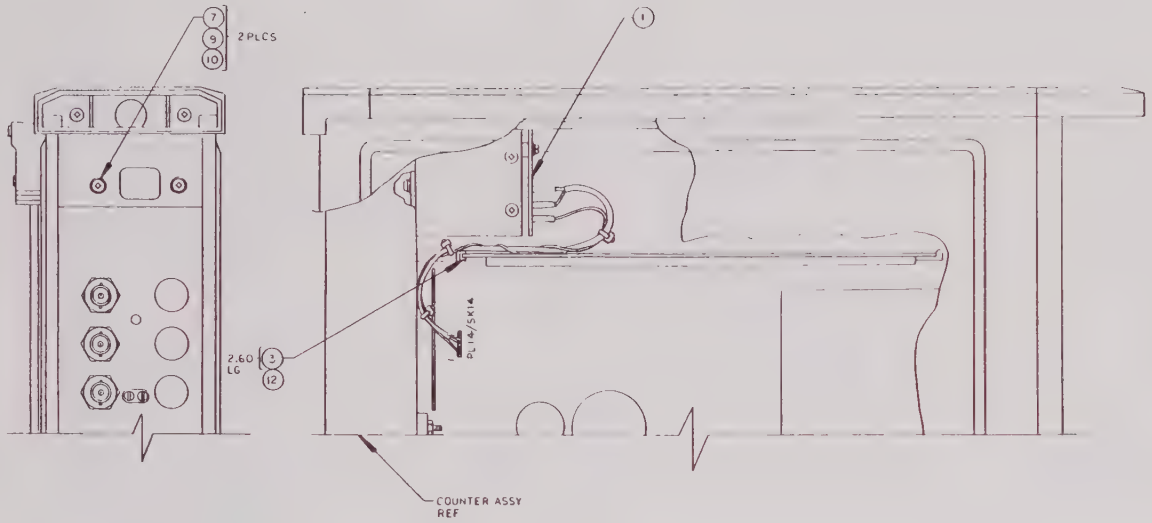
SCALE 1:1 SHEET 1 OF 2

DOC NO 404395



1. REMOVE THE FOLLOWING R/D PART NUMBERS: 10 MHZ OSC. PCB ASSY (401730) & SCREW PPH #4-40 X .312 & WASHER (E1C252) 2 PLCS.

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DOCUMENT TITLE
OSC ASSY, OPTION 04A

SIZE	CODE IDENT NO	DOCUMENT NO	REV
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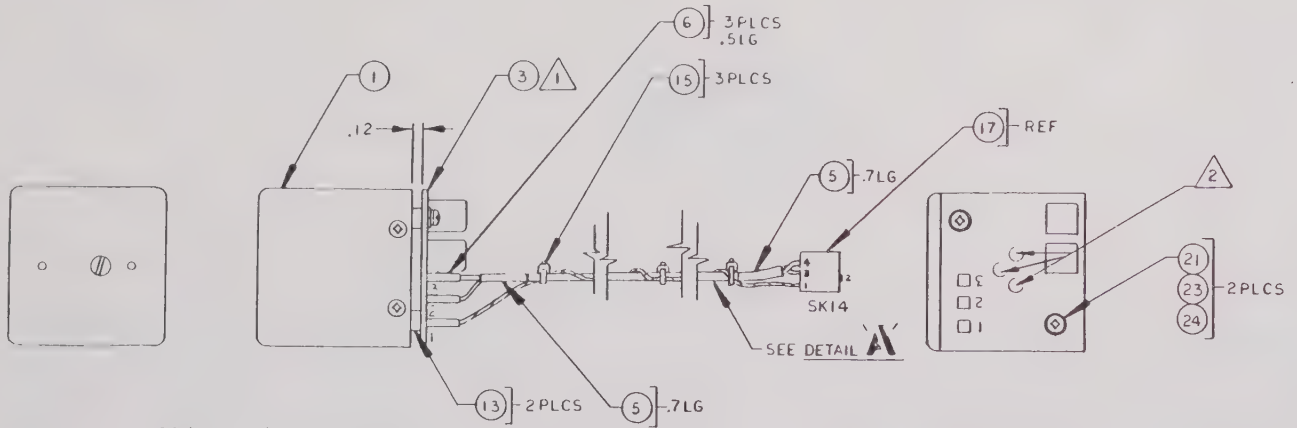
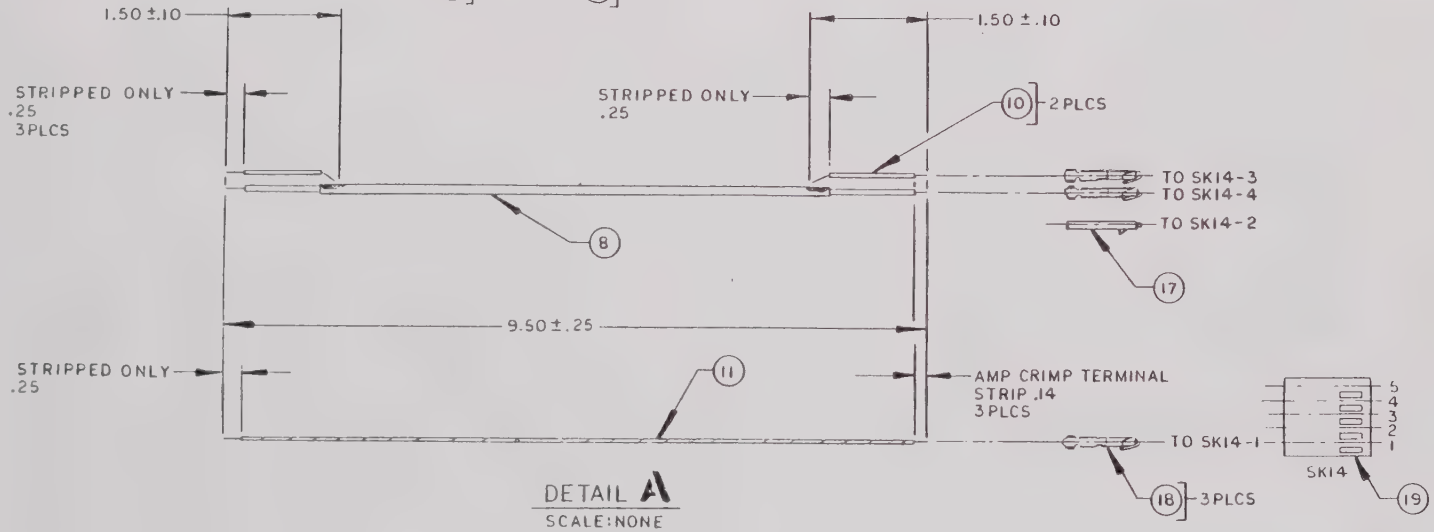
SCALE —— SHEET 1 OF 2

DO NOT SCALE 404392





DETAIL A
SCALE: NONE

2 SOLDER AT ASSY.

1 REMOVE & DISCARD CABLE SUPPLIED WITH ITEM 3 & REPLACE WITH ITEMS 5,6,8,10,11,15, & 17-19.

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DOCUMENT TITLE
OVEN OSCILLATOR, 9444

SIZE	CODE IDENT NO	DOCUMENT NO	REV
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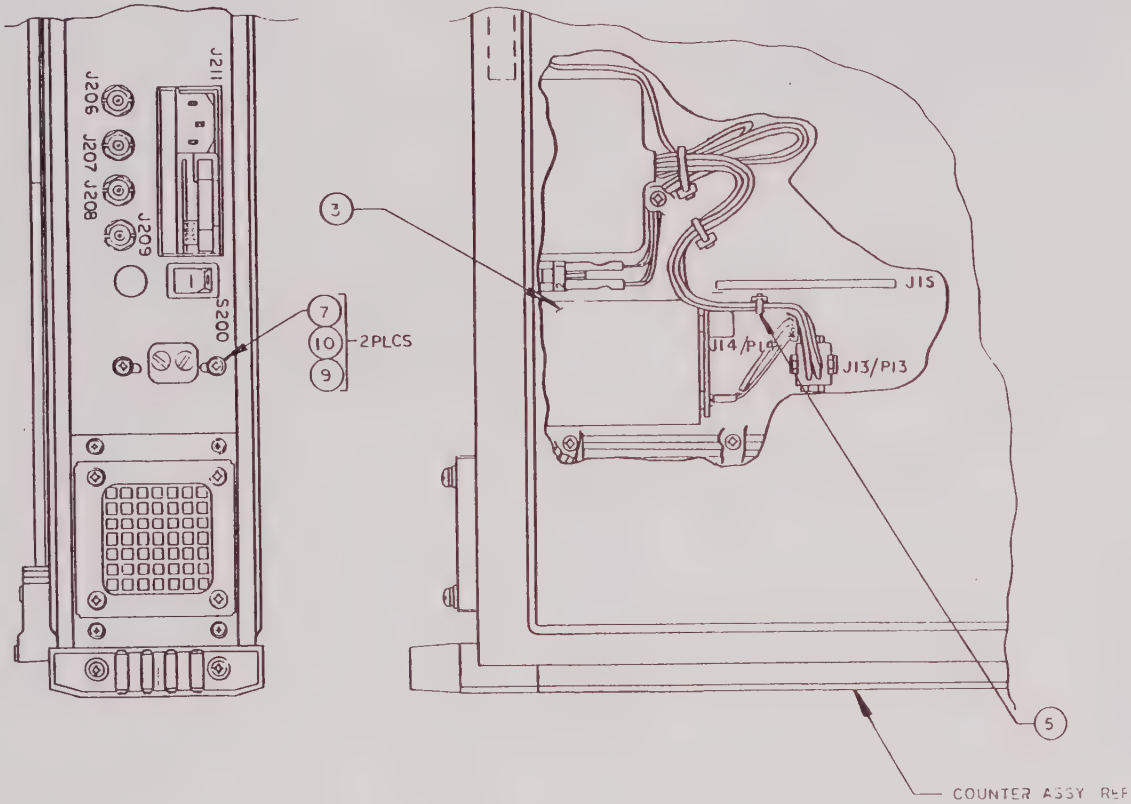
SCALE | SHEET 1 OF 3

DOC NO 404397



2. REMOVE THE FOLLOWING R/D PART NUMBERS: 10MHZ OSC.PCB ASSY(401730) & SCREW PPH #4-40X.312 & WASHER (616252) 2PLCS.
1. REMOVE CABLE TIE (610777) SECURING CABLES TO J14/P14 AND J13/P13.

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DOCUMENT TITLE
OSC ASSY, OPTION 04E

SIZE	CODE IDENT NO	DOCUMENT NO	REV
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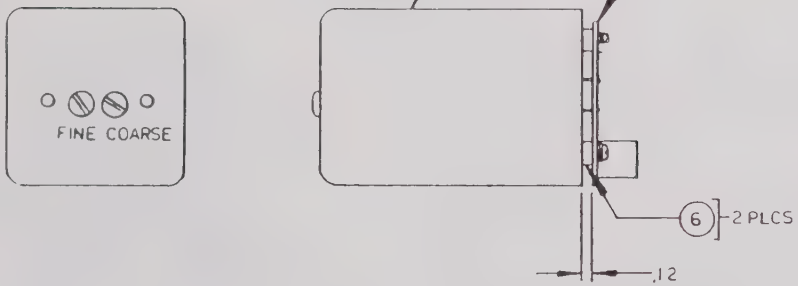
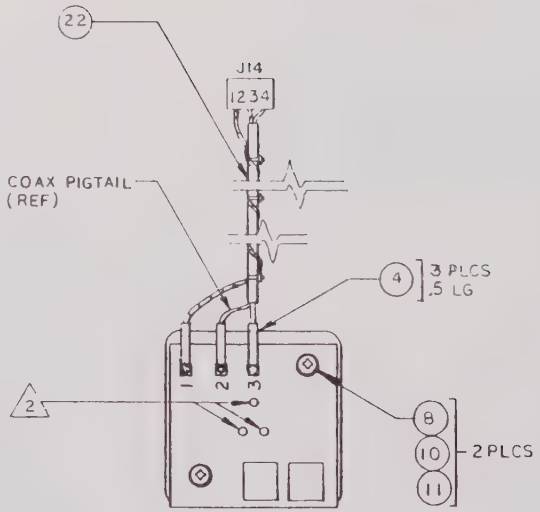
SCALE —— SHEET 1 OF 2

DOC NO 404384





2 SOLDER AT ASSY

1 REMOVE AND DISCARD CABLE SUPPLIED WITH ITEM 1 AND REPLACE WITH CABLE ITEM 22.

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6 GOODYEAR IRVINE CALIFORNIA 92714

DOCUMENT TITLE
OSCILLATOR ASSY

SIZE	CAGE NO.	DOCUMENT NO.	REV
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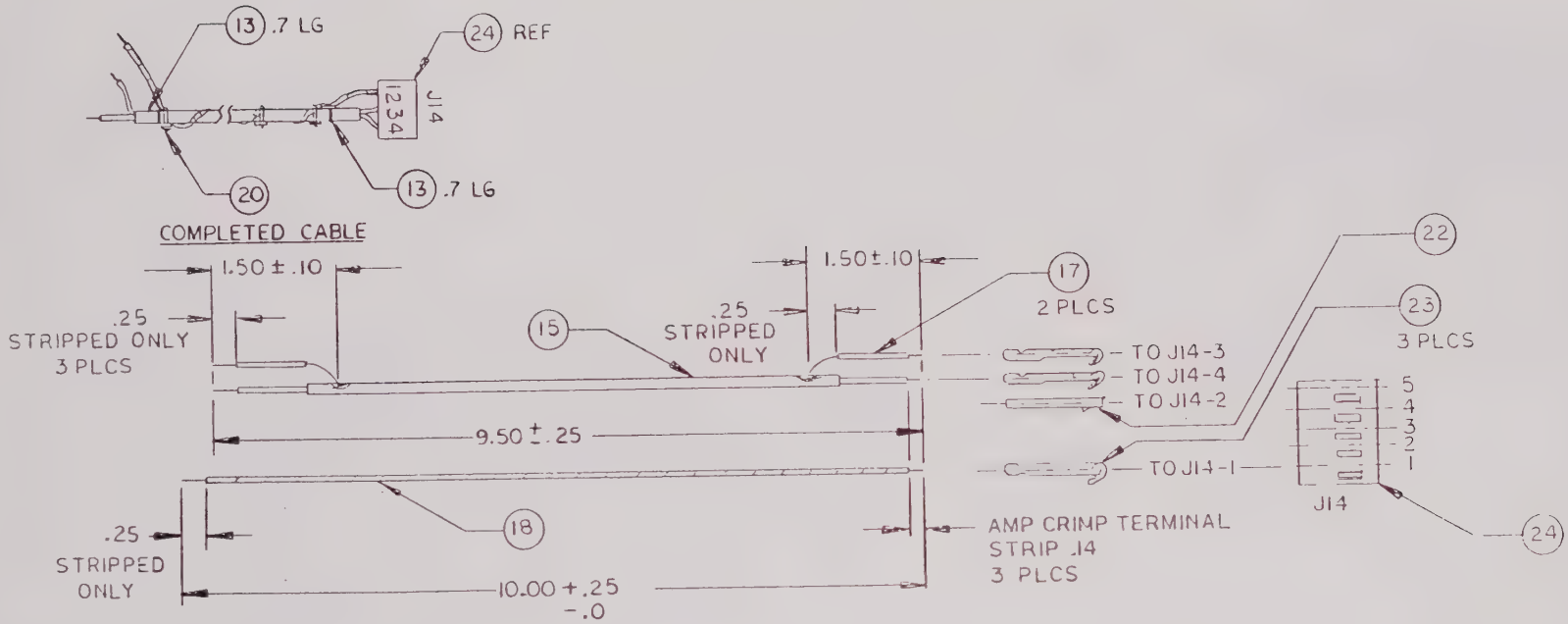
SCALE —— SHEET 1 OF 2



1. PERMANENTLY MARK CABLE WITH RACAL-DANA PART NC. AND CURRENT REV LETTER.

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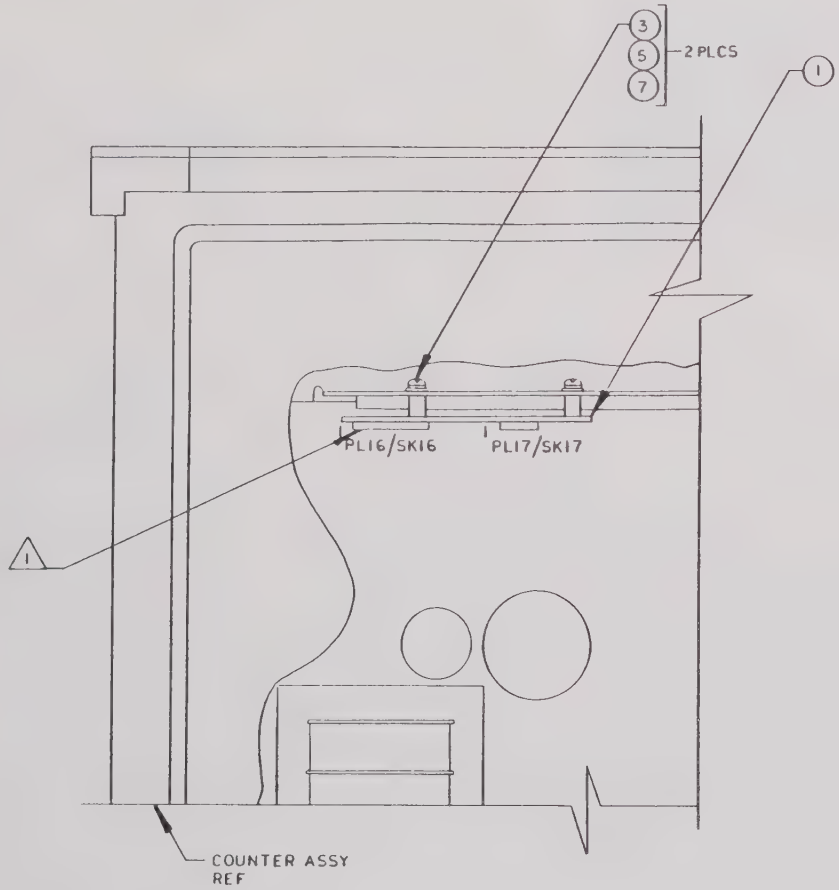
DOCUMENT TITLE

CABLE ASSY, OSC

SIZE	CODE IDENT NO	DOCUMENT NO	REV
B	21793	4C4691	A

SCALE NONE | SHEET 1 OF 2



1 REMOVE JUMPER PLUG NORMALLY FOUND ON PL16 AND DISCARD.

NOTES: UNLESS OTHERWISE SPECIFIED

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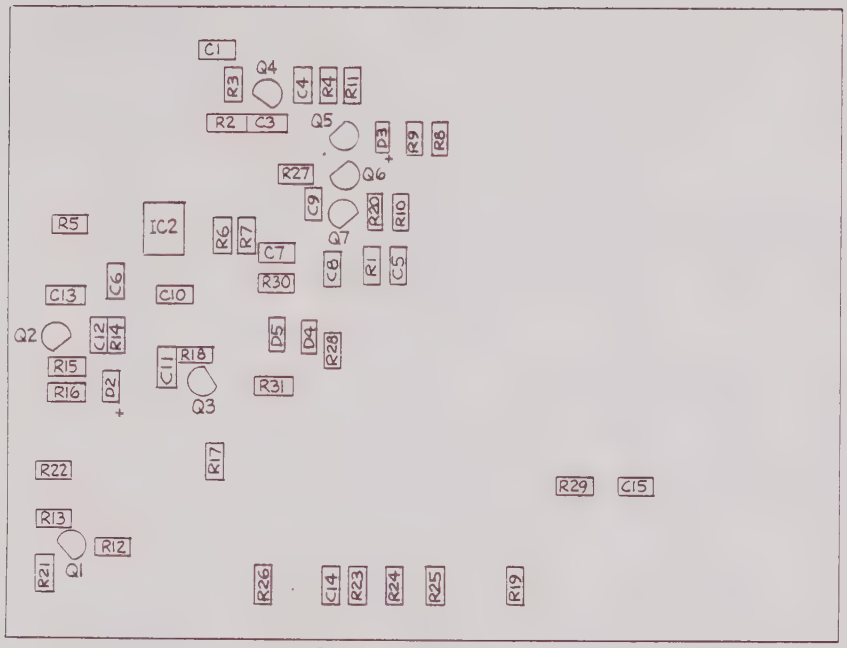
4 GOODYEAR IRVINE CALIFORNIA 92714

DOCUMENT TITLE
REF. MULTIPLIER ASSY, OPTION 10

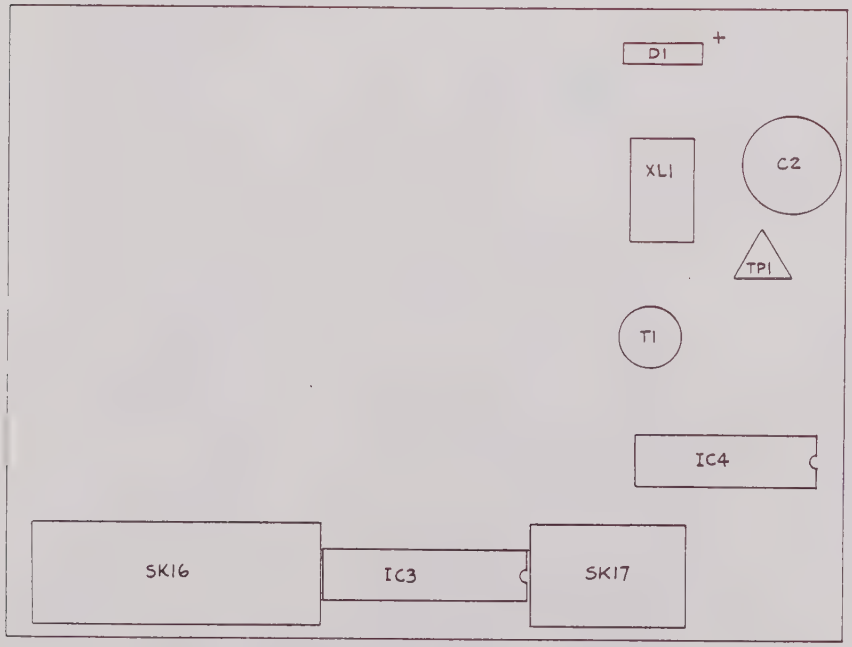
SIZE	CODE IDENT NO.	DOCUMENT NO.	REV
C	21793	404399	A

SCALE —— SHEET 1 OF 2

DOC NO 404399



CIRCUIT SIDE



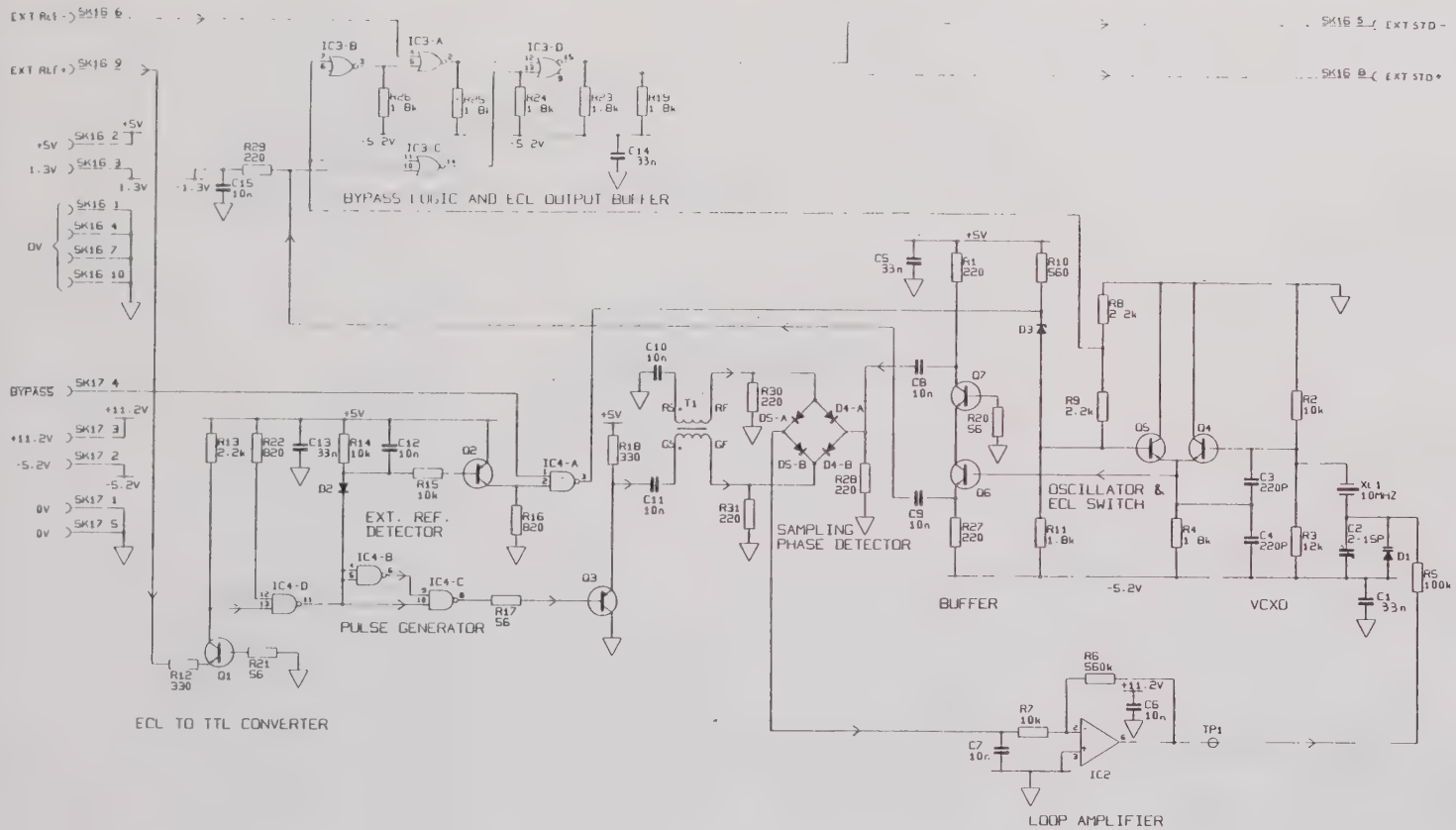
COMPONENT SIDE

RACAL-DANA Instruments Inc.
IRVINE CALIFORNIA

PCB ASSY., REFERENCE FREQUENCY MULTIPLIER

SIZE	CODE IDENT NO	DWG NO	REV
	21793	19-1164	2

SCALE | SHEET 1 OF 1



REFERENCE	PART NO.	TYPE NO.	-5.2V	0V	+5V	+11.2V
D2	22-1053	BA516				
D4,5	22-1096	BAV99				
D1	22-1097	MV1640				
D3	22-1682	BZX84C4V7				
IC2	22-4292	FFC2741UC	4			7
IC3	22-4514	MC10102	8	1,16		
IC4	22-4562	74LS132		7	14	
Q1,4-7	22-6197	FMMT3904				
Q2,3	22-6199	FMMT3906				

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COMPONENT REF
R1-31
C1-15
D1-5
IC2-4
Q1-7
T1
XL1
SK16,17

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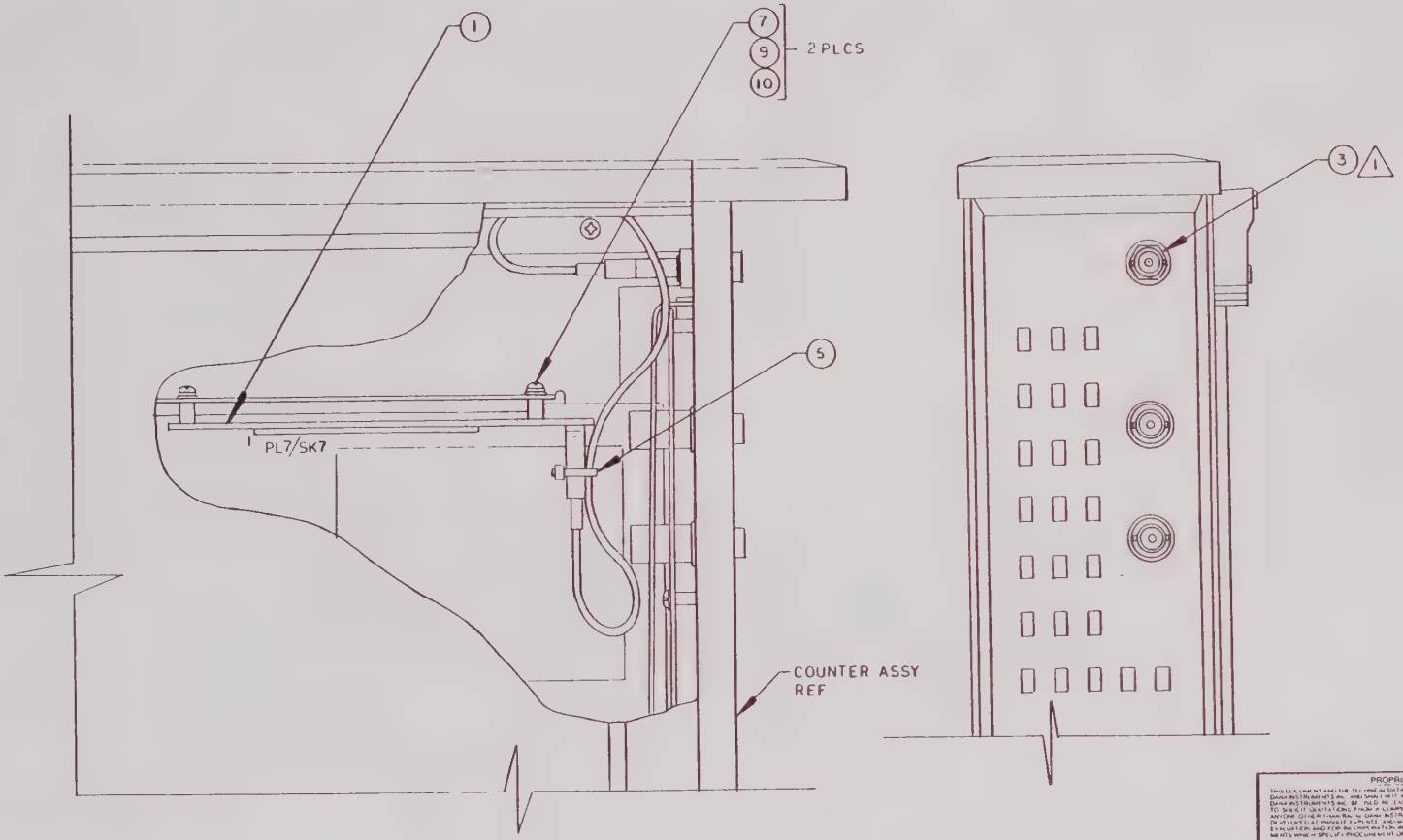
DOCUMENT TITLE
SCHEM, REF MULTIPLIER

SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	432153	A

DATE NONE SHEET 1 OF 1



1 LOCKNUT SUPPLIED WITH BNC ON ITEM 3.

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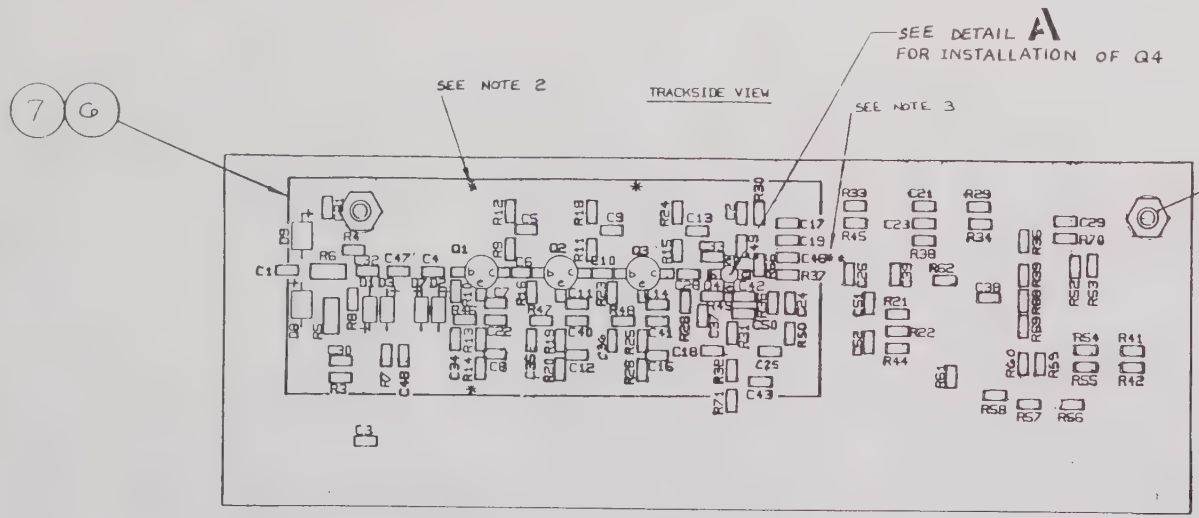
DOCUMENT TITLE
CHANNEL C ASSY, OPTION 41

SIZE	CODE IDENT NO	DOCUMENT NO	REV
C	21793	404398	A

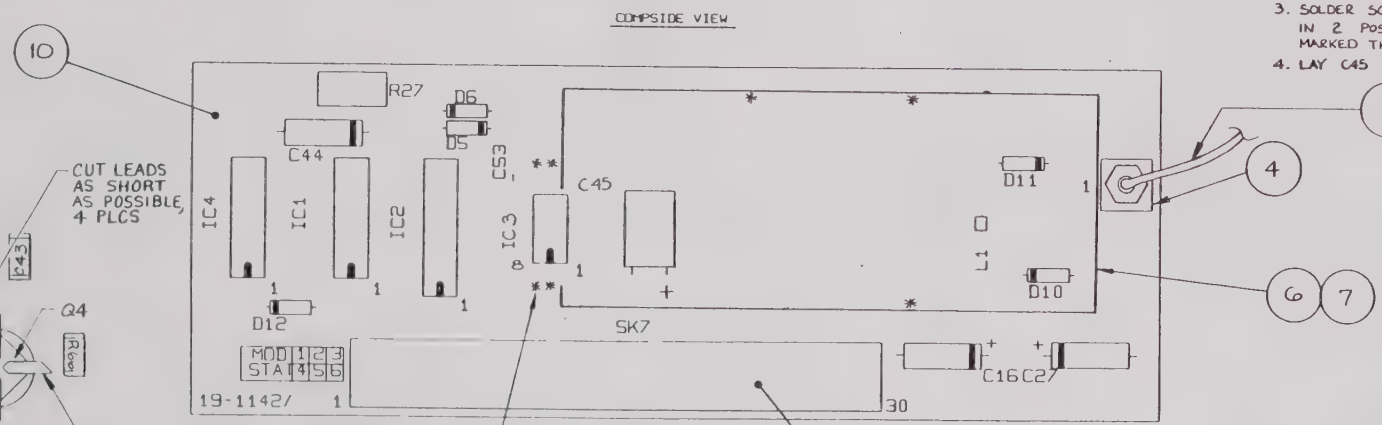
SCALE —— SHEET 1 OF 2

DOC NO 404398



NOTES

1. FIT ITEM 8 2 OFF TO PROTRUDE ON TRACKSIDE
2. FIT WIRE ITEM 166 TO PROTRUDE ON TRACKSIDE AND COMPSIDE AND SOLDER TO ITEMS 5 AND 7 IN 6 POSNS MARKED THUS *
3. SOLDER SCREEN ITEM 6 TO COMPSIDE IN 2 POSNS & TRACKSIDE 1 POSN MARKED THUS * *
4. LAY C45 FLAT ON COMPSIDE



DETAIL A, TRACK SIDE
NO SCALE

1 SEE ZONE C2

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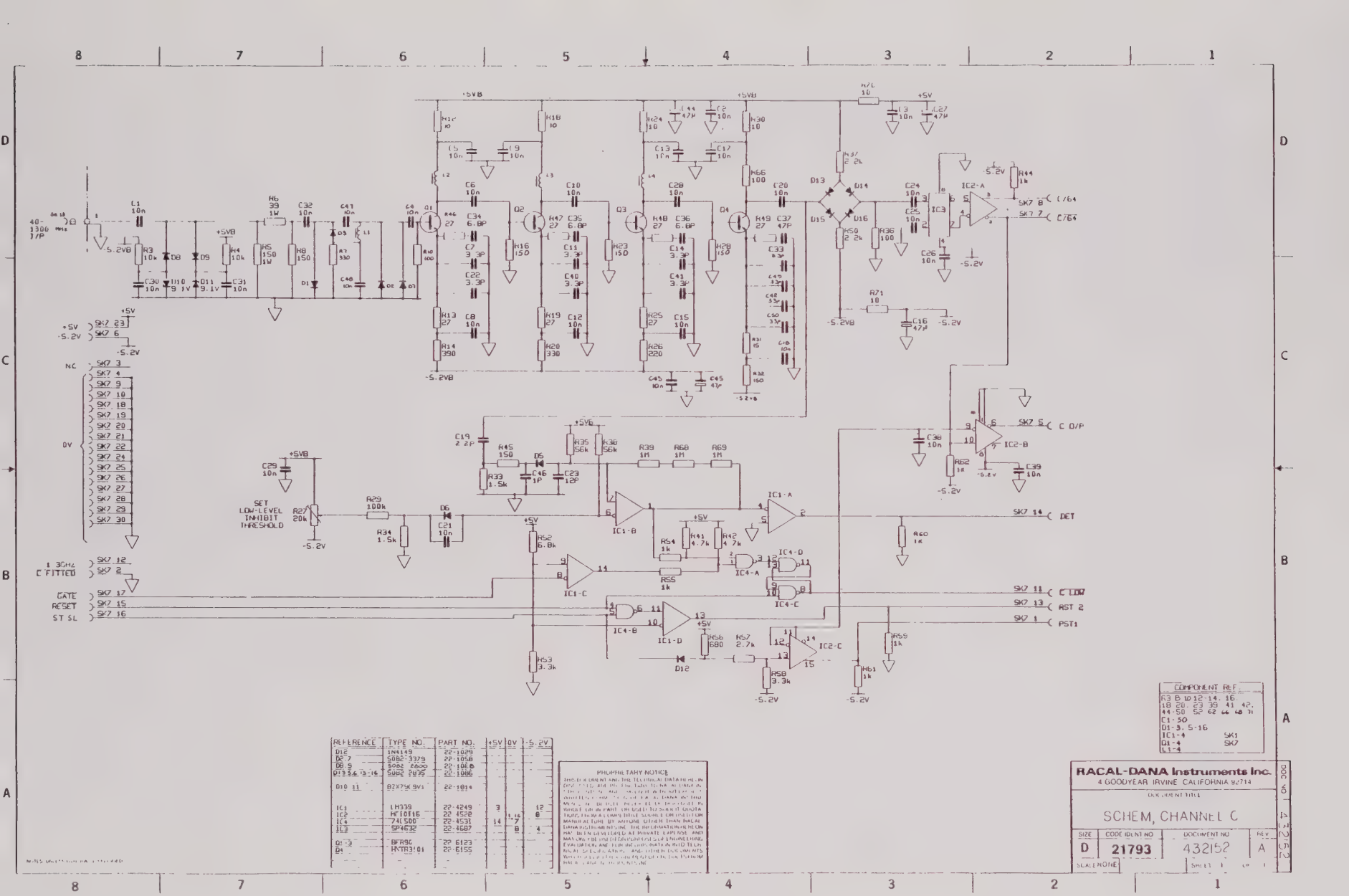
DOCUMENT TITLE
PCB ASSY CHANNEL C

SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	404389	D

SCALE — SHEET 1 OF 6



REFERENCE	TYPE NO.	PART NO.	+5V	0V	-5.2V
D12	1N4149	22-1029			
D2-7	5082-3379	22-1058			
D8,9	5082-2800	22-1068			
D13,14,15,16	5082-2835	22-1086			
D10,11	BZX79C9V1	22-1014			
IC1	LM339	22-4249	3		12
IC2	MC10116	22-4528			8
IC3	741S00	22-4531	14	7	
IC4	SP4632	22-4687		8	4
Q1-3	BFR96	22-6123			
Q4	HXTR3101	22-6155			

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COMPONENT REF
R3 8 10 12-14, 16, 18 20, 23 39 41 42, 44-50 52 62 66 68 71
C1-30
D1-3, 5-16
IC1-4 SK1
D1-4 SK7
L1-4

RACAL-DANA Instruments Inc.
4 GOODYEAR IRVINE CALIFORNIA 92714

DOCUMENT TITLE

SCHEM, CHANNEL C

SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	432152	A

SCALE NONE SHEET 1 OF 1

SECTION 8 PARTS LIST

8.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

404390	Counter Assy	8-3
404391	Chassis Assy	8-3
401730	10 MHz Oscillator	8-4
404426	Motherboard	8-5
401760	GPIB	8-13
401746	Display	8-15
401762	BNC Assy	8-18
401395	Option 01, Rear Input	8-19
404392	Option 04A, Oscillator	8-19
404397	Oscillator Assy	8-20
404384	Option 04E, Oscillator	8-20
404386	Oscillator Assy	8-21
404691	Cable Assy., Oscillator	8-21
404399	Option 10, Reference Frequency Multiplier	8-21
19-1164	Multiplier PCB	8-22
404398	Option 41, Channel C	8-23
404389	Channel C PCB	8-24

8.2 Manufacturers are identified by FSC numbers listed in Table 8.1, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

Table 8.1 - List of Suppliers

FSC	Name
00779	Amp, Inc. Harrisburg, PA
01295	Texas Instruments, Inc. Dallas, TX
02660	Amphenol Corp. Broadview, IL
02735	RCA-Solid State Division Somerville, NJ
03508	General Electric Co. (Semi-Conductor Products Div.) Electronics Park, Syracuse, NY
04713	Motorola, Inc. (Semi-Conductor Division) Phoenix, AZ
05397	Union Carbide Corp. Material Systems Division Cleveland, OH
05972	Locite Corp. Hartford, CT
06383	Panduit Corp. Tinley Park, IL
06540	Amatom Electronic Hardware New Rochelle, NY
07263	Fairchild (Semi-Conductor Division) Mountain View, CA
11236	CTS of Berne, Inc. Berne, IN
11237	CTS Keene, Inc. Pasa Robles, CA
17856	Siliconix, Inc. Santa Clara, CA

FSC	Name
18324	Signetics Corp. Sunnyvale, CA
18677	Scanbe Mfg. Co. El Monte, CA
21793	Racal-Dana Instruments Inc. Irvine, CA
22119	Ferrante Electric Plainview, NY
24022	Teledyne Microwave Mountain View, CA
24226	Gowanda Electronics Corp. Gowanda, NY
25088	Siemens Corp. Components Group Iselin, NJ
27014	National Semi-Conductor Corp. Santa Clara, CA
27264	Molex Products Co. Downers Grove, IL
28520	Heyco Kenilworth, NJ
30146	A P Products, Inc. Planesville, OH
31918	ITT Schadow, Inc. Eden Prarie, MN
32293	Intersil, Inc. Cupertino, CA
34335	Advance Micro Devices Sunnyvale, CA

FSC	Name
50434	Hewlett-Packard Co. HPA Division Palo Alto, CA
50579	Litronix, Inc. Cupertino, CA
52072	Circuit Assembly Corp. Costa Mesa, CA
52648	Plessey Memories Santa Ana, CA
53421	Tyton Corp. Milwaukee, WI
54473	Matsushita Electric Co. Secaucus, NJ
55322	Samtec, Inc. New Albany, IN
58730	Thomas & Betts Co. Elizabeth, NJ
61271	Fujitsu Microelectronics Santa Clara, CA
61802	Toshiba International Houston, TX
70903	Beldon Corp. Chicago, IL
71468	ITT Cannon Electric Santa Ana, CA

FSC	Name
71785	IRW Electronic Components Cinch Division Elk Grove, IL
72982	Erie Technological Products, Inc. Erie, PA
73138	Beckman Instruments, Inc. Fullerton, CA
75915	Littelfuse, Inc. Des Plaines, IL
78189	Illinois Tool Works, Inc. Shakeproof Division Elgin, IL
80294	Bourns, Inc. Riverside, CA
81349	Military Specification
83330	Herman H. Smith, Inc. Brookyn, NY
91506	Augut, Inc. Attleboro, MA
91637	Dale Electronics, Inc. Columbus, NE
95275	Vitramon, Inc. Bridgeport, CT
95987	Weckesser Co., Inc. Chicago, IL

404390 - COUNTER ASSEMBLY A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	404391	CHASSIS ASSY.	21793	404391
3	404108	COVER ASSY., BOTTOM	21793	404108
5	454319	FOOT, REAR (2 REQ'D)	21793	454319
7	454385	PANEL, COVER, TOP	21793	454385
8	454386	PANEL, SIDE COVER (2 REQ'D)	21793	454386
10	454393	HANDLE ASSY. (2 REQ'D)	21793	454393
12	454859	OVERLAY, FRONT PANEL	21793	454859
13	454865	OVERLAY, REAR PANEL	21793	454865
15	600620	CABLE, POWER, AC LINE	70903	KHS-7041
17	610231	BUTTON, PLUG, PLASTIC (4 REQ'D)	28520	P-500
18	610379	WASHER, NYLON, FLAT, #4, (4 REQ'D)	95987	NW4-2812
19	615073	SCREW, PPH, 8-32 X .312 (4 REQ'D)	---	---
21	610925	SCREW, PPH, 6-32 X 1 (4 REQ'D)	78189	---
23	920888	LABEL, IDENTIFICATION	21793	920888

404391 - CHASSIS ASSEMBLY E

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	401730	PCB ASSY., 10 MHZ OSC.	21793	401730
2	R-18-1161	PCB, VOLTAGE SELECTOR	21793	R-18-1161
3	401746	PCB ASSY., DISPLAY	21793	401746
5	401760	PCB ASSY., GPIB	21793	401760
6	401762	PCB ASSY., BNC	21793	401762
7	404426	PCB ASSY., MOTHERBOARD	21793	404426
8	454390	BLOCK, MOUNTING (6 REQ'D)	21793	454390
10	454863	PANEL, FRONT	21793	454863
11	454864	PANEL, REAR	21793	454864
12	454866	PLATE, SUPPORT, BOTTOM	21793	454866
13	454882	PANEL, SIDE (2 REQ'D)	21793	454882
14	454900	SHIELD, HIGH VOLTAGE	21793	454900
15	500064	TUBING, SHRINK, .09 ID	---	---
17	500132	WIRE, TEFLON, STRANDED, 24 GA, TWISTED PAIR, BLK/WHT	---	---
18	524000	WIRE, TEFLON STRANDED, 24 GA, WHT	---	---
19	600808	CONNECTOR, BNC	02660	31-010
20	600032	LUG, SOLDER, INT. TOOTH, #4	83330	1416-4
21	600961	CABLE CLIP, ADHESIVE MOUNT (2 REQ'D)	06383	ACC19-A-C
22	610027	GROMMET, RUBBER, 3/16 ID, BLK	83330	2172
23	601248	CABLE ASSY., 14-PIN (2 REQ'D)	55322	1DSD-7-D-7.5-RS
24	610410	CABLE CLAMP, SELF-LOCK	58730	TY-33M
25	610777	CABLE TIE (2 REQ'D)	53421	T18R
26	610909	SCREW, PPH, 6-32 X .50 (6 REQ'D)	---	---
27	610899	TIE, CABLE, SELF LOCKING, 1/16" - 2"	58730	Y-232M
28	616255	SCREW, PPH, SEMS ASSY., 6-32 X .312 (6 REQ'D)	78189	---
29	610820	WASHER, SHOULDER, TO-220 (3 REQ'D)	13103	14875

404391 - CHASSIS ASSEMBLY (CONT'D) E

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
30	611053	TERMINAL, CRIMP (2 REQ'D)	00779	530553-2
31	611054	CONNECTOR, CABLE, 2-PIN	00779	530554-1
32	611069	CARD GUIDE, .06 X 6.0 LG	18677	23071-5
33	611070	CARD GUIDE, .06 X 8.0 LG	18677	11633-6
34	611071	STANDOFF, M/F, M4 (2 REQ'D)	06540	19955-B-3560
35	611072	SPACER, BNC (2 REQ'D)	21793	611072
36	610851	WASHER, INSULATING, TIP-32 (3 REQ'D)	18565	60-11-5791-1674
37	616252	SCREW, PPH, SEMS ASSY., 4-40 X .312 (12 REQ'D)	78189	---
38	616257	SCREW, PPH, SEMS ASSY., 6-32 X .500 (6 REQ'D)	78189	---
39	611088	SCREW, M3.5 X 0.6 X 4 M (2 REQ'D)	21793	611088
40	617004	NUT, HEX, 4-40 (4 REQ'D)	---	---
41	617103	WASHER, FLAT, LIGHT SERIES, #6 (2 REQ'D)	---	---
42	617017	NUT, HEX (RADIO), 6-32 (2 REQ'D)	---	---
43	617127	WASHER, LOCK, LIGHT SERIES, #4	---	---
44	617128	WASHER, LOCK, LIGHT SERIES, #6 (2 EQ'D)	---	---
45	617077	WASHER, INTERNAL LOCK, #4 (3 REQ'D)	---	---
46	920729	LABEL, WARNING	21793	920729
47	615044	SCREW, PPH, 4-40 X .375 (3 REQ'D)	---	---
48	921021	BUTTON, RED, .5 DIA	21793	921021

401730 - PCB ASSY., 10 MHZ OSCILLATOR A

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG.P/N
P14	611056	CONNECTOR, CABLE, 5 PIN	00779	530554-4
Y1	921013	OSCILLATOR, 10 MHZ	21793	921013
1	411730	PCB, 10 MHZ OSCILLATOR (UNLOADED)	21793	411730
4	524211	WIRE, TEFLON, STRANDED, 24 GA, BRN/RED	---	---
5	524333	WIRE, TEFLON, STRANDED, 24 GA, ORG	---	---
6	524555	WIRE, TEFLON, STRANDED, 24 GA, GRN	---	---
8	610160	STANDOFF, 4-40, THRU SWAGE (2 REQ'D)	83330	4103
10	610777	CABLE TIE	53421	18TR
12	611052	KEY, POLARIZING, PLUG	00779	87077-1
13	611053	TERMINAL, CRIMP (4 REQ'D)	00779	530553-2

404426, MOTHERBOARD PCB ASSY. 4

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG P/N
C1	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C2	21-1801	CAP,CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C3	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C4	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C5	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C6	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C7	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C8	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C9	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C10	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C11	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C12	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C13	21-1800	CAP, CHIP, 1 NF, 50V, 10%	95275	VJ1206Y102MF
C14	21-1800	CAP, CHIP, 1 NF, 50V, 10%	95275	VJ1206Y102MF
C22	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C23	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C24	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C25	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C26	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C27	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C28	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C35	21-1800	CAP, CHIP, 1 NF, 50V, 10%	95275	VJ1206Y102MF
C36	21-1847	CAP, CHIP, 20 NF, 400V, 10%	95275	VJ1206Y203MF
C37	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF

404426, MOTHERBOARD PCB ASSY (CONT'D) 4

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C40	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C41	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C42	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C43	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C44	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C45	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C46	21-7003	CAP, POLY, 47 NF, 250V, 20%	25088	B81121-C-123
C47	21-7002	CAP, POLY, 2.5 NF, 250V, 20%	25088	B81121-C-B141
C48	21-7002	CAP, POLY, 2.5 NF, 250V, 20%	25088	B81121-C-B141
C49	21-0683	CAP, ELECT., 10,000 UF, 16V	18324	222205055103
C50	21-0667	CAP, ELECT., 4700 UF, 16V, -10 + 30%	18324	222205055472
C52	21-0797	CAP, ELECT., 680 UF, 25V, 20%	21793	21-0797
C53	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C54	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C55	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C56	21-1838	CAP, CHIP, 220 PF, 50V, 5%	95275	VJ1206A221JF
C57	21-1838	CAP, CHIP, 220 PF, 50V, 5%	95275	VJ1206A221JF
C58	21-1838	CAP, CHIP, 220 PF, 50V, 5%	95275	VJ1206A221JF
C59	21-0797	CAP, ELECT., 680 UF, 25V, 20%	21793	21-0797
C65	21-1847	CAP, CHIP, 20 NF, 400V, 10%	95275	VJ1206Y203MF
C66	21-1847	CAP, CHIP, 20 NF, 400V, 10%	95275	VJ1206Y203MF
C67	21-1859	CAP, CHIP, 6.8 PF, 400V, 10%	21793	21-1859
C68	21-1862	CAP, CHIP, 47 PF, 50V, 2%	95275	VJ1206A470GXA
C69	21-1859	CAP, CHIP, 6.8 PF, 400V, 10%	21793	21-1859

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C70	21-1862	CAP, CHIP, 47 PF, 50V, 2%	95275	VJ1206A470GXA
C71	21-1780	CAP, CHIP, 2.7 PF	95275	VJ1206A2R7CF
C72	21-1782	CAP, CHIP, 3.9 PF	95275	VJ1206A3R9CF
C73	21-1857	CAP, CHIP, 100 PF, 400V, 10%	95275	VJ1206Y101MF
C74	21-1857	CAP, CHIP, 100 PF, 400V, 10%	95275	VJ1206Y101MF
C75	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C76	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C77	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C78	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C79	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C80	21-1802	CAP, CHIP, 100 NF, 50V, 10%	95275	VJ1206Y104MF
C81	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C82	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C83	100133	CAP, CERAM, .1 MFD, L.P., 20%	72982	8131LP-100-651-104M
C84	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C85	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C86	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C87	21-1858	CAP, CHIP, 3.3 NF, 50V, 10%	95275	VJ1206Y332KF
C88	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C89	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C90	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C91	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C92	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C93	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C94	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C95	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C96	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C97	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C98	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C99	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C100	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C101	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C102	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C103	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C104	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C105	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C106	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C107	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C108	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C109	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C110	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C111	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C112	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C113	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C114	21-0779	CAP, ELECT., 1 UF, 50V, 20%	54473	ECEA1HK1R0E
C115	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C116	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C117	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C118	21-1800	CAP, CHIP, 1 NF, 50V, 10%	95275	VJ1206Y102MF
C119	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C120	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C121	21-0779	CAP, ELECT., 1 UF, 50V, 20%	54473	ECEA1HK1R0E
C125	110249	CAP, ELECT, 220 UF, 10V, 20%	55680	ULBA221M
C126	21-0779	CAP, ELECT., 1 UF, 50V, 20%	54473	ECEA1HK1R0E
C127	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y2103MF
C128	21-1800	CAP, CHIP, 1 NF, 50V, 10%	95275	VJ1206Y102MF
C129	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C130	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C131	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C132	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C133	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C225	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
C226	21-0789	CAP, ELECT., 47 UF, 25V, 20%	18324	035-56479
D1	22-1029	DIODE, SILICO	01295	1N4149
D2	22-1029	DIODE, SILICO	01295	1N4149
D3	22-1029	DIODE, SILICO	01295	1N4149
D5	22-1099	DIODE, SILICO	17856	JPAD50
D6	22-1029	DIODE, SILICO	01295	1N4149
D7	22-1029	DIODE, SILICO	01295	1N4149
D8	22-1099	DIODE, SILICO	17856	JPAD50
D11	22-1662	BRIDGE, RECTIFIER	21793	22-1662

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
D12	22-1664	BRIDGE, DIODE	21793	22-1664
D13	22-1029	DIODE, SILICO	01295	1N4149
D14	22-1029	DIODE, SILICO	01295	1N4149
D15	22-1029	DIODE, SILICO	01295	1N4149
D18	210089	DIODE, HOT CARRIER	50434	2835
D19	210089	DIODE, HOT CARRIER	50434	2835
D20	210089	DIODE, HOT CARRIER	50434	2835
D21	210089	DIODE, HOT CARRIER	50434	2835
D22	210089	DIODE, HOT CARRIER	50434	2835
D23	210089	DIODE, HOT CARRIER	50434	2835
D24	210089	DIODE, HOT CARRIER	50434	2835
D25	210089	DIODE, HOT CARRIER	50434	2835
D26	22-1029	DIODE, SILICO	01295	1N4149
D28	22-1029	DIODE, SILICO	01295	1N4149
D30	22-1801	DIODE	71468	BZX79C2V7
D31	22-1801	DIODE	71468	BZX79C2V7
D32	22-1809	DIODE	01295	BZX79C5V6
D33	22-1809	DIODE	01295	BZX79C5V6
F1	920204	FUSE, SLO, 0.5A, 250V	75915	3AG1/2ASB
F2	920756	FUSE, SLO-BLO, 1/4A, 250V (FOR 240V OPER.)	75915	MDL1/4
FS1	23-0062	FUSE HOLDER	21793	23-0062
FS1	23-0063	FUSE HOLDER, TOP	21793	23-0063
H1	230791	HYBRID TEC	21793	230791
H2	17-1035	HYBRID DAC	21793	17-1035

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
IC1	230750	IC, DIGITAL, ECL	04713	MC10216P
IC2	230787	IC, DIGITAL, TRIPLE LINE REC'R	04713	MC10116P
IC3	230200	IC, 12 VDC REGULATOR	04713	MC7812CT
IC4	230201	IC, NEG 12V 3-TERMINAL REGULATOR	04713	MC7912-CP
IC14	230787	IC, DIGITAL, TRIPLE LINE REC'R	04713	MC10116P
IC18	230790	IC, MCC1, CUSTOM	21793	230790
IC19	22-8307	IC, 8-BIT CMOS MICROPROCESSOR	04713	MC146803E2
IC20	230806	IC, OCTAL TRANSPARENT LATCH, 3-STATE OUTPUT	02735	74HCT373E
IC21	230368	IC, DEMULTIPLEXER	27014	74LS138
IC22*	230822	IC, EPROM, 32K X 8	21793	230822
IC23	22-4807	IC, OCTAL BUFFER/LINE DRIVER, 3-STATE	01295	74HGT244
IC24	230561-001	IC, OCTAL LATCH	04713	SN74LS373N
IC25	230806	IC, OCTAL TRANSPARENT LATCH	02735	74LS373E
IC26	230194	IC, DUAL D FLIP-FLOP	01295	SN74LS373N
IC27	230428	IC, QUAD 2-INPUT OR GATE	27014	DM74LS74N
IC28	230248	IC, POSITIVE NAND GATE	01295	SN74LS10N
IC29	230234	IC, HEX INVERTER	01295	NS74LS04N
IC30	230466	IC, CMOS QUAD NAND GATE	02735	CD4011UBE
IC31	22-4262	IC, QUAD OR AMP	07263	MC3403
IC32	22-4756	IC, HEX SCHMITT TRIGGERS	18324	40106

*When ordering a replacement for IC22 and IC39, it is essential that the software issue number and the serial number of the instrument are quoted in addition to the part number. The software issue number is marked on the component.

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
IC34	22-4269	IC, MOS/FET INPUT, BIPOLAR, OUTPUT OR AMP	02735	CA3140E
IC35	22-4269	IC, MOS/FET INPUT, BIPOLAR, OUTPUT OR AMP	02735	CA3140E
IC36	230735	IC, COMPARATOR, DUAL ULTRA FAST	52648	SP9687DG
IC39*	230789	IC, DIGITAL, ECL/TTL CHIP	21793	230789
IC41	230733	IC, DIGITAL, ECL FLIP-FLOP	04713	MC10231
L1	23-7217	CHOKE, 40 UH	21793	23-7217
L2	23-7217	CHOKE, 40 UH	21793	23-7217
L5	310151	CHOKE, 100 UH	91637	IR-2
L6	310151	CHOKE, 100 UH	91637	IR-2
L7	310151	CHOKE, 100 UH	91637	IR-2
L8	310151	CHOKE, 100 UH	91637	IR-2
L9	310151	CHOKE, 100 UH	91637	IR-2
L10	310151	CHOKE, 100 UH	91637	IR-2
L11	310151	CHOKE, 100 UH	91637	IR-2
L14	310152	CHOKE, WIDEBAND	02114	VK200-10/3B
L15	310152	CHOKE, WIDEBAND	02114	VK200-10/3B
L20	310151	CHOKE, 100 UH	91637	IR-2
LK1	601195	PLUG, JUMPER, 0.1 CTR, L.P.	00779	531220-2
LK2	600245	JUMPER, INSULATED	55210	L-2007-1LP
LK3	600245	JUMPER, INSULATED	55210	L-2007-1LP
LK4	601195	PLUG, JUMPER, 0.1 CTR, L.P.	00779	531220-2

*When ordering a replacement for IC22 and IC39, it is essential that the software issue number and the serial number of the instrument are quoted in addition to the part number. The software issue number is marked on the component.

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
PL1	601251	CONNECTOR, PCB, PLUG, 14 PIN	52072	CA-D14SP100-230T-530
PL2	601251	CONNECTOR, PCB, PLUG, 14 PIN	52072	CA-D14SP100-230T-530
PL7	601208-013	CONNECTOR, PCB, PLUG, 30 PIN	52072	CA-S-30-SP100-230-430
PL14	601208-012	CONNECTOR, PCB, PLUG, 5 PIN	52072	CA-S-5-SP100-230-430
PL15	601208-016	CONNECTOR, PCB, PLUG, 3 PIN	52072	CA-S-03-SP100-230-430
PL16	601208-015	CONNECTOR, PCB, PLUG, 10 PIN	52072	CA-S-10-SP100-230-430
PL17	601208-012	CONNECTOR, PCB, PLUG, 5 PIN	52072	CA-S-5-SP100-230-430
PL18	601208-012	CONNECTOR, PCB, PLUG, 5 PIN	52072	CA-S-5-SP100-230-430
PL19	23-5176	PLUG, 2 X 3-WAY	21793	23-5176
PL20	23-5161	PLUG, REAR BNC BOARD, 2 X 2-WAY	27264	10-90-1041
PL50	601208-018	CONNECTOR, PCB, PLUG, 13 PIN	52072	CA-S-13-SP100-230-430
Q1	22-6018	TRANSISTOR, PNP	07263	MPS3640
Q2	22-6018	TRANSISTOR, PNP	07263	MPS3640
Q3	22-6018	TRANSISTOR, PNP	07263	MPS3640
Q4	200298	TRANSISTOR, NPN	04713	2N3904
Q7	22-6113	TRANSISTOR, PNP	22119	ZTX550
Q9	22-6112	TRANSISTOR, NPN	22119	ZTX450
Q10	22-6112	TRANSISTOR, NPN	22119	ZTX450
Q11	200298	TRANSISTOR, NPN	04713	2N3904
Q13	22-6113	TRANSISTOR, PNP	22119	ZTX550
Q14	200298	TRANSISTOR, NPN	04713	2N3904
Q15	22-6163	TRANSISTOR, N CH, FET	25088	BF256A
Q16	22-6163	TRANSISTOR, N CH, FET	25088	BF256A

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
Q17	22-6206	TRANSISTOR, BFS 17	21793	22-6206
Q18	22-6206	TRANSISTOR, BFS 17	21793	22-6206
Q21	22-6206	TRANSISTOR, BFS17	21793	22-6206
Q22	200298	TRANSISTOR, NPN	04713	2N3904
Q23	22-6206	TRANSISTOR, BFS17	21793	22-6206
Q24	200298	TRANSISTOR, NPN	04713	2N3904
Q25	200299	TRANSISTOR, PNP	04713	2N3906
Q26	200299	TRANSISTOR, PNP	04713	2N3906
Q27	200299	TRANSISTOR, PNP	04713	2N3906
Q28	22-6113	TRANSISTOR, PNP	22119	ZTX550
Q29	22-4216	TRANSISTOR ARRAY, HIGH CURRENT, NPN	02735	CA3083
R1	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R2	20-5541	RES, COM. SIL, 1K X 9, 10P	80294	4310R-101-102
R3	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R4	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R5	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R6	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R7	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R8	20-5771	RES, CHIP, 10 OHM, 1/8W, 5%	18324	RC-01
R11	20-5765	RES, CHIP, 470 OHM, 1/8W, 5%	18324	RC-01
R16	20-5765	RES, CHIP, 470 OHM, 1/8W, 5%	18324	RC-01
R18	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R25	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R32	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R33	20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	18324	RC-01
R35	20-5799	RES, CHIP, 4.7K, 1/8W, 5%	18324	RC-01
R40	20-5799	RES, CHIP, 4.7K, 1/8W, 5%	18324	RC-01
R45	000391	RES, CARBON, 390 OHM, 1/4W, 5%	81349	RC07GF391J
R46	20-5562	RES, SEP. SIL, 10K X 5, 10P	80294	4310R-102-103
R47	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R48	000121	RES, CARBON, 120 OHM, 1/4W, 5%	81349	RC07GF121J
R49	20-5556	RES, CUSTOM ARRAY, SIL	21793	20-5556
R54	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R60	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R63	000391	RES, CARBON, 390 OHM, 1/4W, 5%	81349	RC07GF391J
R65	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R67	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R68	20-5813	RES, CHIP, 100K, 1/8W, 5%	18324	RC-01
R69	000391	RES, CARBON, 390 OHM, 1/4W, 5%	81349	RC07GF391J
R75	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R76	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R77	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R78	001675	RES, CARBON, 100 OHM, 1/2W, 5%	81349	RC20GF101J
R79	001675	RES, CARBON, 100 OHM, 1/2W, 5%	81349	RC20GF101J
R80	001675	RES, CARBON, 100 OHM, 1/2W, 5%	81349	RC20GF101J
R81	001675	RES, CARBON, 100 OHM, 1/2W, 5%	81349	RC20GF101J
R82	010990	RES, METAL, 900K, 1/2W, .1%	81349	RN65C9003B

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R83	010989	RES, METAL, 111K, 1/8W, .1%	81349	RN55C1113B
R84	010990	RES, METAL, 900K, 1/2W, .1%	81349	RN65C9003B
R85	010989	RES, METAL, 111K, 1/8W, .1%	81349	RN55C1113B
R87	20-5554	RES, CUSTOM ARRAY, SIL	21793	20-5554
R88	20-5554	RES, CUSTOM ARRAY, SIL	21793	20-5554
R89	20-5554	RES, CUSTOM ARRAY, SIL	21793	20-5554
R91	20-5554	RES, CUSTOM ARRAY, SIL	21793	20-5554
R93	20-5817	RES, CHIP, 560K, 1/8W, 5%	18324	RC-01
R94	20-5784	RES, CHIP, 180 OHM, 1/8W, 5%	18324	RC-01
R95	20-5817	RES, CHIP, 560K, 1/8W, 5%	18324	RC-01
R96	20-5784	RES, CHIP, 180 OHM, 1/8W, 5%	18324	RC-01
R97	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R98	20-5765	RES, CHIP, 470 OHM, 1/8W, 5%	18324	RC-01
R100	20-5793	RES, CHIP, 1.2K, 1/8W, 5%	18324	RC-01
R101	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R102	20-5765	RES, CHIP, 470 OHM, 1/8W, 5%	18324	RC-01
R104	20-5793	RES, CHIP, 1.2K, 1/8W, 5%	18324	RC-01
R107	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R110	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R111	20-5771	RES, CHIP, 10 OHM, 1/8W, 5%	18324	RC-01
R112	20-5771	RES, CHIP, 10 OHM, 1/8W, 5%	18324	RC-01
R113	20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	18324	RC-01
R115	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01

404426, MOTHERBOARD PCB ASSY (CONT'D) 4

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R116	20-5765	RES, CHIP, 470 OHM, 1/8W, 5%	18324	RC-01
R117	20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	18324	RC-01
R119	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R120	20-5765	RES, CHIP, 470 OHM, 1/8W, 5%	18324	RC-01
R121	20-5796	RES, CHIP, 2.2K, 1/8W, 5%	18324	RC-01
R122	20-5796	RES, CHIP, 2.2K, 1/8W, 5%	18324	RC-01
R123	20-5796	RES, CHIP, 2.2K, 1/8W, 5%	18324	RC-01
R124	20-5796	RES, CHIP, 2.2K, 1/8W, 5%	18324	RC-01
R125	20-5790	RES, CHIP, 680 OHM, 1/8W, 5%	18324	RC-01
R126	20-5790	RES, CHIP, 680 OHM, 1/8W, 5%	18324	RC-01
R128	20-5785	RES, CHIP, 220 OHM, 1/8W, 5%	18324	RC-01
R129	20-5794	RES, CHIP, 1.5K, 1/8W, 5%	18324	RC-01
R135	20-5813	RES, CHIP, 100K, 1/8W, 5%	18324	RC-01
R136	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R137	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R139	000100	RES, CARBON, 10 OHM, 1/4W, 5%	81349	RC07GF100J
R140	20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	18324	RC-01
R141	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R142	20-5780	RES, CHIP, 68 OHM, 1/8W, 5%	18324	RC-01
R143	000100	RES, CARBON, 10 OHM, 1/4W, 5%	72982	RC07GF100J
R144	20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	18324	RC-01
R145	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R146	20-5771	RES, CHIP, 10 OHM, 1/8W, 5%	18324	RC-01
R147	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01

404426, MOTHERBOARD PCB ASSY (CONT'D) 4

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R148	20-5797	RES, CHIP, 3.3K, 1/8W, 5%	18324	RC-01
R149	20-7071	POT, 10K	80294	3386F
R150	20-7071	POT, 10K	80294	3386F
R151	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R152	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R155	20-5799	RES, CHIP, 4.7K, 1/8W, 5%	18324	RC-01
R156	20-5799	RES, CHIP, 4.7K, 1/8W, 5%	18324	RC-01
R157	20-5813	RES, CHIP, 100K, 1/8W, 5%	18324	RC-01
R158	20-5799	RES, CHIP, 4.7K, 1/8W, 5%	18324	RC-01
R159	20-5763	RES, CHIP, 18 OHM, 1/8W, 5%	18324	RC-01
R160	20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	18324	RC-01
R161	20-5780	RES, CHIP, 68 OHM, 1/8W, 5%	18324	RC-01
R163	20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	18324	RC-01
R164	20-5780	RES, CHIP, 68 OHM, 1/8W, 5%	18324	RC-01
R165	20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	18324	RC-01
R166	20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	18324	RC-01
R167	20-5797	RES, CHIP, 3.3K, 1/8W, 5%	18324	RC-01
R168	20-5797	RES, CHIP, 3.3K, 1/8W, 5%	18324	RC-01
R169	20-5778	RES, CHIP, 47 OHM, 1/8W, 5%	18324	RC-01
R170	000121	RES, CARBON, 120 OHM, 1/4W, 5%	81349	RC07GF121J
R171	000121	RES, CARBON, 120 OHM, 1/4W, 5%	81349	RC07GF121J
R174	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R175	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R177	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R178	20-5797	RES, CHIP, 3.3K, 1/8W, 5%	18324	RC-01
R179	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R180	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R181	20-5765	RES, CHIP, 470 OHM, 1/8W, 5%	18324	RC-01
R186	20-5817	RES, CHIP, 560K, 1/8W, 5%	18324	RC-01
R187	20-5817	RES, CHIP, 560K, 1/8W, 5%	18324	RC-01
R188	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R189	20-5806	RES, CHIP, 27K, 1/8W, 5%	18324	RC-01
R190	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R191	20-5806	RES, CHIP, 27K, 1/8W, 5%	18324	RC-01
R192	20-7071	POT, 10K	80294	3386F
R193	20-7071	POT, 10K	80294	3386F
R194	20-5771	RES, CHIP, 10 OHM, 1/8W, 5%	18324	RC-01
R195	20-5774	RES, CHIP, 22 OHM, 1/8W, 5%	18324	RC-01
R196	20-5784	RES, CHIP, 180 OHM, 1/8W, 5%	18324	RC-01
R198	20-5771	RES, CHIP, 10 OHM, 1/8W, 5%	18324	RC-01
R199	20-5774	RES, CHIP, 22 OHM, 1/8W, 5%	18324	RC-01
R200	20-5784	RES, CHIP, 180 OHM, 1/8W, 5%	18324	RC-01
R202	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R203	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R204	20-5799	RES, CHIP, 4.7K, 1/8W, 5%	18324	RC-01
R205	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R206	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R207	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R208	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R209	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R210	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R211	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R212	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R213	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R214	20-5796	RES, CHIP, 2.2K, 1/8W, 5%	18324	RC-01
R215	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R216	20-5780	RES, CHIP, 68 OHM, 1/8W, 5%	18324	RC-01
R217	20-5813	RES, CHIP, 100K, 1/8W, 5%	18324	RC-01
R218	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R219	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R220	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R221	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R222	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R223	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R224	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R225	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R226	20-5780	RES, CHIP, 68 OHM, 1/8W, 5%	18324	RC-01
R227	20-5771	RES, CHIP, 10 OHM, 1/8W, 5%	18324	RC-01
R228	20-5792	RES, CHIP, 1K, 1/8W, 5%	18324	RC-01
R229	20-5796	RES, CHIP, 2.2K, 1/8W, 5%	18324	RC-01

404426, MOTHERBOARD PCB ASSY (CONT'D)

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
RLA	23-7529	RELAY, REED	21793	23-7529
RLB	23-7529	RELAY, REED	21793	23-7529
RLC	23-7529	RELAY, REED	21793	23-7529
RLD	23-7529	RELAY, REED	21793	23-7529
RLE	23-7530	RELAY, DIL	21793	23-7530
RLF	23-7528	RELAY, REED	21793	23-7528
RLG	23-7528	RELAY, REED	21793	23-7528
RLH	23-7527	RELAY, DPDT	24022	172-5
SK4	23-3290	SOCKET, IC, 28-WAY	21793	23-3290
SK5	601234	CONN, BNC, PCB MOUNT	21793	601234
SK6	601234	CONN, BNC, PCB MOUNT	21793	601234
SK8	23-5156	SOCKET, MAINS SELECTOR	27264	2184-68
SK10	23-3429	SOCKET, MAINS	21793	23-3429
S1	601259	SWITCH, POWER, DPDT	31918	MSA-M
T1	17-4102	TRANSFORMER	21793	17-4102
386	920891	SOCKET, IC,28-WAY (2 REQ'D)	52072	CA-28S-TSD
388	611059	CONN, DIP, LO PROFILE, 40P (3 REQ'D)	91506	240-AG39D

401760 - PCB ASSY., GPIB

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
BAT	921026	BATTERY, NI-CAD, 3.6V, 63 MAH	03508	DS3GT
C1	110181	CAP, TANTA, 47 MFD, 25V	05397	T36D476025A
C2	100133	CAP, CERAM, .1 MFD, LOW PROFILE 20%	72982	8131LP-100-651-104M
C3	100133	CAP, CERAM, .1 MFD, LOW PROFILE 20%	72982	8131LP-100-651-104M
C4	100133	CAP, CERAM, .1 MFD, LOW PROFILE 20%	72982	8131LP-100-651-104M
C5	100133	CAP, CERAM, .1 MFD, LOW PROFILE 20%	72982	8131LP-100-651-104M
C6	100133	CAP, CERAM, .1 MFD, LOW PROFILE 20%	72982	8131LP-100-651-104M
C7	100133	CAP, CERAM, .1 MFD, LOW PROFILE 20%	72982	8131LP-100-651-104M
C8	100133	CAP, CERAM, .1 MFD, LOW PROFILE 20%	72982	8131LP-100-651-104M
C9	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C10	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
CR1	211083	DIODE, SILICO	81349	1N916B
IC1	230802	IC, OCTAL D-TYPE F-F, 3-STATE	02735	74HCT374
IC2	230802	IC, OCTAL D-TYPE F-F, 3-STATE	02735	74HCT374
IC3	230710	IC, DIGITAL, DECODER	07263	74F138
IC4	230801	IC, HEX BUFFERS/DRIVERS	04713	7407
IC5	230105	IC, TRI-STATE BUFFER	01295	SN7417
IC6	230805	IC, QUAD 2-INPUT NOR GATE	02735	74HCT02

401760 - PCB ASSY., GPIB (CONT'D)

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
IC7	230796	IC, QUAD 2-INPUT NAND GATE	02735	74HCT00E
IC8	230797	IC, 3 TO 8 LINE DECODER/DEMULTIPLEXER	02735	74HCT138E
IC9	230821	IC, CPU, CMOS, 64K, EXT MEMORY	04713	MC146805E3P
IC10	230814	IC, GPIB PROM	21793	230814
IC11	230806	IC, OCTAL TRANSPARENT LATCH, 3-STATE OUTPUT	02735	74HCT373E
IC12	230430	IC, GPIA	04713	MC68488L
IC13	230247	IC, MOS BILATERAL SWITCH	02735	CD4066AD
IC14	230472	IC, OCTAL GPIB TRANS	01295	SN75161
IC15	230459	IC, OCTAL GPIB TRANS	01295	SN75160
IC16	230798	IC, DUAL D W/SET & RESET	02735	74HCT74E
IC17	230798	IC, DUAL D W/SET & RESET	02735	74HCT74E
IC18	230796	IC, QUAD 2-INPUT NAND GATE	02735	74HCT00E
IC19	230805	IC, QUAD 2-INPUT NOR GATE	02735	74HCT02
IC20	230804	IC, QUAD 2-INPUT OR GATE	02735	74HCT32
IC21	230802	IC, OCTAL D-TYPE F-F, 3-STATE	02735	74HCT374
IC22	230802	IC, OCTAL D-TYPE F-F, 3-STATE	02735	74HCT374
IC23	230515	IC, VOLTAGE DETECTOR, MICROPOWER	32293	ICL8212CPA
IC24	230795	IC, MEMORY	21793	230795
IC25	230798	IC, DUAL D W/SET & RESET	02735	74HCT74E
IC26	230803	IC, QUAD 2-INPUT EXCLUSIVE OR GATE	02735	74HCT86
IC27	230804	IC, QUAD 2-INPUT OR GATE	02735	74HCT32
IC28	230795	IC, MEMORY	21793	230795
Q1	200299	TRANS, PNP	04713	2N3906

401760 - PCB ASSY., GPIB (CONT'D)

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R1	080082	RES NETWORK, 9 X 3.3K	11236	750-101-R3.3K
R2	000560	RES, CARBON, 56 OHM, 1/4W, 5%	81349	RC07GF560J
R3	080082	RES NETWORK, 9 X 3.3K	11236	750-101-R3.3K
R4	000331	RES, CARBON, 330 OHM, 1/4W, 5%	81349	RC07GF331J
R5	000331	RES, CARBON, 330 OHM, 1/4W, 5%	81349	RC07GF331J
R6	000331	RES, CARBON, 330 OHM, 1/4W, 5%	81349	RC07GF331J
R7	080024	RES NETWORK, CERMET, 3.3K, 6P/5R, 2%	11236	750-61-R3.3K OHM
R8	000180	RES, CARBON, 18 OHM, 1/4W, 5%	81349	RC07GF180J
R9	000560	RES, CARBON, 56 OHM, 1/4W, 5%	81349	RC07GF560J
R10	000331	RES, CARBON, 330 OHM, 1/4W, 5%	81349	RC07GF331J
R11	000472	RES, CARBON, 4.7K, 1/4W, 5%	81349	RC07GF472J
R12	000472	RES, CARBON, 4.7K, 1/4W, 5%	81349	RC07GF472J
R13	010643	RES, METAL, 71.5K, /18W, 1%	81349	RN55C7152F
R14	000304	RES, CARBON, 300K, 1/4W, 5%	81349	RC07GF304J
R15	010697	RES, METAL, 26.7K, 1/8W, 1%	81349	RN55C2672F
R16	000181	RES, CARBON, 180 OHM, 1/4W, 5%	81349	RC07GF181J
R17	080057	RES NETWORK, 100K, 2%	11236	750-81-R100K OHM
R18	080057	RES NETWORK, 100K, 2%	11236	750-81-R100K OHM
R19	000472	RES, CARBON, 4.7K, 1/4W, 5%	81349	RC07GF472J
SK1	920891	SOCKET, 28P, SOLDER TAIL	52072	CA-28S-TSD
SK2	601249	CONNECTOR, DIP, RIGHT ANGLE, 14-PIN	52072	CA-14SE-10RAC3-01

401760 - PCB ASSY., GPIB (CONT'D)

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
SK3	601253	CONNECTOR, GPIB, 24-PIN	00779	553811-3
SW1	600814	SWITCH, SLIDE, 6 SPST	11237	206-6
TP1,2	601208-010	CONNECTOR, PCB, PLUG	21793	601208-010
57	411760	PCB, GPIB (UNLOADED)	21793	411760
59	600947	SOCKET, IC, 20-PIN (5-REQ'D)	52072	CA-20S-TSD-BC
63	404472	CABLE ASSY.	21793	404472
64	601247	CABLE ASSY., 28-PIN	52072	CA-D28P02-281-TT-002
66	610777	CABLE TIE (3 REQ'D)	53421	T18R
68	920734	SOCKET, IC, 14-PIN	00779	583527-1
69	611059	CONNECTOR, DIP, LOW PROFILE, 40P (2 REQ'D)	91506	240-AG39D
70	616252	SCREW, PPH, SEMS ASSY., 4-40 X .312 (2 REQ'D)	78189	---
71	920735	SOCKET, IC, 16-PIN	71785	133-51-02-006
72	630010	HARDWARE KIT, STANDOFF, STUD MOUNT	00779	552633-3
73	920624	SOCKET, IC, 24-PIN (2 REQ'D)	71785	133-59-02-063
74	920891	SOCKET, 28-PIN, SOLDERTAIL	52072	CA-28S-TSD

401746 - PCB ASSY., DISPLAY C

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C3	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C4	110163	CAP, TANTA, 4.7 MFD, 35V, 20%	05397	T368B475M035AS
C5	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
CR1	211083	DIODE, SILICO	81349	1N916B
CR2	211083	DIODE, SILICO	81349	1N916B
CR3	211083	DIODE, SILICO	81349	1N916B
CR4	211083	DIODE, SILICO	81349	1N916B
CR5	211083	DIODE, SILICO	81349	1N916B
DS1	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS2	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS3	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS4	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS5	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS6	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS7	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS8	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS9	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS10	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
LD1	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD2	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122

401746 - PCB ASSY., DISPLAY (CONT'D) C

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
LD3	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD4	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD5	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD6	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD7	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD8	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD9	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD10	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD11	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD12	210106	DIODE, LIGHT EMITTING; RED	25088	LDH1112
LD13	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD14	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD15	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD16	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD17	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD18	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD19	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD20	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD21	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD22	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD23	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD24	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD25	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD26	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122

401746 - PCB ASSY., DISPLAY (CONT'D) C

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
LD27	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD28	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD29	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD30	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD31	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD32	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD33	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD34	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD35	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD36	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD37	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD38	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
LD39	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD40	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD41	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD42	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD43	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD44	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD45	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD46	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
LD47	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
S1	601211	SWITCH, PUSHBUTTON	21793	601211
S2	601211	SWITCH, PUSHBUTTON	21793	601211
S3	601211	SWITCH, PUSHBUTTON	21793	601211

401746 - PCB ASSY., DISPLAY (CONT'D) C

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
S4	601211	SWITCH, PUSHBUTTON	21793	601211
S5	601211	SWITCH, PUSHBUTTON	21793	601211
S6	601211	SWITCH, PUSHBUTTON	21793	601211
S7	601211	SWITCH, PUSHBUTTON	21793	601211
S8	601211	SWITCH, PUSHBUTTON	21793	601211
S9	601211	SWITCH, PUSHBUTTON	21793	601211
S10	601211	SWITCH, PUSHBUTTON	21793	601211
S11	601211	SWITCH, PUSHBUTTON	21793	601211
S12	601211	SWITCH, PUSHBUTTON	21793	601211
S13	601211	SWITCH, PUSHBUTTON	21793	601211
S14	601211	SWITCH, PUSHBUTTON	21793	601211
S15	601211	SWITCH, PUSHBUTTON	21793	601211
S16	601211	SWITCH, PUSHBUTTON	21793	601211
S17	601211	SWITCH, PUSHBUTTON	21793	601211
S18	601211	SWITCH, PUSHBUTTON	21793	601211
S19	601211	SWITCH, PUSHBUTTON	21793	601211
S20	601211	SWITCH, PUSHBUTTON	21793	601211
S21	601211	SWITCH, PUSHBUTTON	21793	601211
S22	601211	SWITCH, PUSHBUTTON	21793	601211
S23	601211	SWITCH, PUSHBUTTON	21793	601211
S24	601211	SWITCH, PUSHBUTTON	21793	601211
S25	601211	SWITCH, PUSHBUTTON	21793	601211
S26	601211	SWITCH, PUSHBUTTON	21793	601211
S27	601211	SWITCH, PUSHBUTTON	21793	601211

401746 - PCB ASSY., DISPLAY (CONT'D) C

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
S28	601211	SWITCH, PUSHBUTTON	21793	601211
S29	601211	SWITCH, PUSHBUTTON	21793	601211
S30	601211	SWITCH, PUSHBUTTON	21793	601211
S31	601211	SWITCH, PUSHBUTTON	21793	601211
S32	601211	SWITCH, PUSHBUTTON	21793	601211
S33	601211	SWITCH, PUSHBUTTON	21793	601211
S34	601211	SWITCH, PUSHBUTTON	21793	601211
S35	601211	SWITCH, PUSHBUTTON	21793	601211
S36	601211	SWITCH, PUSHBUTTON	21793	601211
S37	601211	SWITCH, PUSHBUTTON	21793	601211
S38	601211	SWITCH, PUSHBUTTON	21793	601211
S39	601211	SWITCH, PUSHBUTTON	21793	601211
S40	601211	SWITCH, PUSHBUTTON	21793	601211
SK1	601250	CONNECTOR, 14P RT. ANGLE DUAL ROW CONNECTOR	52072	CA-D14R5P100-230T-190
SK2	601250	CONNECTOR, 14P RT. ANGLE DUAL ROW CONNECTOR	52072	CA-D14R5P100-230T-190
U1	230809	IC, 20 KEY ENCODER	27014	MM74C923
U2	230819	IC, CMOS QUAD AND GATE	27014	CD4081BCN
U3	230457	IC, LED DRIVER	50579	ICM7218A
U4	230457	IC, LED DRIVER	50579	ICM7218A
Z1	080058	RES NETWORK, CERMET, 15K, 10P9R	11236	750-101-R15K
Z2	080058	RES NETWORK, CERMET, 15K, 10P9R	11236	750-101-R15K

401746 - PCB ASSY., DISPLAY (CONT'D) C

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
17	411746	PCB, DISPLAY (UNLOADED)	21793	411746
20	454817-021	SPACER, LED, 3 POS. MOD	21793	454817-021
21	454817-024	SPACER, LED, 6 POS. MOD	21793	454817-024
27	921007	CAP, SWITCH, GRAY (25 REQ'D)	21793	921007
29	921009	CAP, SWITCH, BLUE	21793	921009
31	921049-01	CAP, SWITCH, "1"	21793	921049-01
32	921049-02	CAP, SWITCH, "2"	21793	921049-02
33	921049-03	CAP, SWITCH, "3"	21793	921049-03
34	921049-04	CAP, SWITCH, "4"	21793	921049-04
35	921049-05	CAP, SWITCH, "5"	21793	921049-05
36	921049-06	CAP, SWITCH, "6" (2 REQ'D)	21793	921049-06
37	921049-07	CAP, SWITCH, "7"	21793	921049-07
38	921049-08	CAP, SWITCH, "8"	21793	921049-08
39	921049-09	CAP, SWITCH, "0"	21793	921049-09
40	921049-010	CAP, SWITCH, "."	21793	921049-010
41	921049-011	CAP, SWITCH, "EXP"	21793	921049-011
42	921049-012	CAP, SWITCH, "CE"	21793	921049-012
43	921049-013	CAP, SWITCH, "+/-"	21793	921049-013

401762 - PCB ASSY., BNC D

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C2	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C3	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C6	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
CR1	220012	DIODE, SILICO, ZENER	81349	1N958B
CR2	220012	DIODE, SILICO, ZENER	81349	1N958B
R2	001730	RES, CARBON, 470 OHM, 5%, 1/2W	81349	RC20GF471J
R3	000471	RES, CARBON, 470 OHM, 5%, 1/4W	81349	RC07GF471J
R5	040247	POT, CERMET, 5K, 20%, 1/2W	73138	72PX5K
R6	000272	RES, CARBON, 2.7K, 5%, 1/4W	81349	RC07GF272J
R8	000823	RES, CARBON, 82K, 5%, 1/4W	81349	RC07GF823J
R9	000272	RES, CARBON, 2.7K, 5%, 1/4W	81349	RC07GF272J
R10	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF101J
SK3	601254-050	CONNECTOR, BNC SOCKET, MODIFIED	21793	601254-050
SK4	601254	CONNECTOR, BNC SOCKET	21793	601254
SK5	601254	CONNECTOR, BNC SOCKET	21793	601254
SK19	601520	CONNECTOR, PCB, 6-PIN	30146	929975-01-03
SK20	601255	CONNECTOR, 4-WAY SOCKET	30146	929975-07
U1	230445	IC, 686 VOLTAGE COMPARATOR	34335	AM686CN-1
W1	500023	WIRE, BARE COPPER/TIN, 24 GA	---	---
20	24-3547	TERMINAL (2 REQ'D)	21793	24-3547
22	411762	PCB, BNC (UNLOADED)	21793	411762

404395 - OPTION 01, REAR INPUT A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	601235	CONNECTOR, BNC, PNL MTG	21793	601235
3	601258	CABLE ASSY., COAX (2 REQ'D)	21793	601258
5	610777	CABLE TIE	53421	T18R

404392 - OPTION 04A, OSCILLATOR ASSY. A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	404397	OVEN OSCILLATOR	21793	404397
3	610389	GROMMET, CATERPILLAR, .063 THK	---	---
7	611067	SCREW, METRIC, M3 X 8 (2 REQ'D)	---	---
9	617102	WASHER, FLAT, #4, LIGHT SERIES (2 REQ'D)	---	---
10	617127	WASHER, LOCK, #4, LIGHT SERIES (2 REQ'D)	---	---
12	920962	LOCTITE, 242, MED. STR.	05972	242

404397 - OVEN OSCILLATOR B

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
SK14	611056	CONNECTOR, CABLE, 5-PIN	21793	611056
1	11-1710	OSCILLATOR	21793	11-1710
3	401822	PCB ASSY., DOUBLER	21793	401822
5	500009	TUBING, SHRINK, .125 ID, BLK	---	---
6	500064	TUBING, SHRINK, .01 ID	---	---
8	500174	CABLE, COAX, LOW THERMAL	---	---
10	524555	WIRE, TEFLON, STRANDED, 24GA, GRN	---	---
11	524929	WIRE, TEFLON, STRANDED, 24GA, WHT/RED	---	---
13	610304	SPACER, 1/4D X 1/2 LG (2 REQ'D)	---	---
15	610777	CABLE TIE (3 REQ'D)	53421	T18R
17	611052	KEY, POLARIZING, PLUG	00779	87077-1
18	611053	TERMINAL, CRIMP (3 REQ'D)	00779	530553-2
21	611074	SCREW, METRIC, M3 X 10 (2 REQ'D)	---	---
23	617102	WASHER, FLAT, #4, LIGHT SERIES (2 REQ'D)	---	---
24	617127	WASHER, LOCK, #4, LIGHT SERIES (2 REQ'D)	---	---

404384 - OPT. 04E, OSCILLATOR

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
3	404386	OSCILLATOR ASSY.	21793	404386
5	610777	CABLE TIE	53421	T18R
7	611067	SCREW, METRIC, M3 X 8 (2 REQ'D)	---	---
9	617102	WASHER, FLAT, #4, LIGHT SERIES (2 REQ'D)	---	---
10	617127	WASHER, LOCK, #4, LIGHT SERIES (2 REQ'D)	---	---

404386 - OSCILLATOR ASSY. (OPT. 04E) D

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	401822	PCB ASSY., DOUBLER	21793	401822
2	454879	FREQUENCY STD., 5 MHZ	21793	454879
4	500064	TUBING, SHRINK, .093 ID	---	---
6	610304	SPACER, 1/4D X 1/2 LG (2 REQ'D)	---	---
8	611074	SCREW, METRIC, M3 X 10 (2 REQ'D)	---	---
10	617102	WASHER, FLAT, #4, LIGHT SERIES (2 REQ'D)	---	---
11	617127	WASHER, LOCK, #4, LIGHT SERIES (2 REQ'D)	---	---
22	404691	CABLE ASSY., OSCILLATOR	21793	404691

404691 - CABLE ASSY., OSCILLATOR A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
13	500009	TUBING, SHRINK, .125 ID, BLK	29005	RNF-100-1-1/8
15	500174	CABLE, COAX, LOW THERMAL	21793	500174
17	524555	WIRE, TEFLON, STRANDED, 24 GA, GRN	---	---
18	524929	WIRE, TEFLON, STRANDED, 24 GA, WHT/RED	---	---
20	610777	CABLE TIE (3 REQ'D)	53421	T18R
22	611052	KEY, POLARIZING, PLUG	00779	87077-1
23	611053	TERMINAL, CRIMP (3 REQ'D)	00779	530553-2
24 J14	611056	CONNECTOR, CABLE, 5-PIN	21793	611056

404399 - OPTION 10, REF. FREQUENCY MULTIPLIER A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	19-1164	PCB ASSY., MULTIPLIER	21793	19-1164
3	611067	SCREW, METRIC, M3 X 8 (2 REQ'D)	---	---
5	617102	WASHER, FLAT, #4, LIGHT SERIES (2 REQ'D)	---	---
7	617127	WASHER, LOCK, #4, LIGHT SERIES (2 REQ'D)	---	---

19-1164, REFERENCE FREQUENCY MULTIPLIER ASSY 2

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C2	21-6043	CAP, TRIMMER, 2-15P	18324	2222-808-11159
C3	21-1838	CAP, CHIP, 220 PF, 50V, 10%	95275	VJ1206A221JF
C4	21-1838	CAP, CHIP, 220 PF, 50V, 10%	95275	VJ1206A221JF
C5	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C6	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C7	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C8	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C9	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C10	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C11	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C12	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
C13	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C14	21-1808	CAP, CHIP, 33 NF, 50V, 10%	95275	VJ1206Y333MF
C15	21-1801	CAP, CHIP, 10 NF, 50V, 10%	95275	VJ1206Y103MF
D1	22-1097	DIODE, VARACTOR, 39P AT 4V	04713	MV1640
D2	22-1093	DIODE, HIGH SPEED	22119	HD3A
D3	22-1882	DIODE, ZENER, 4.7V	22119	BZX84-C4V7
D4	22-1096	DIODE, DUAL, BAV99	18324	BAV99
D5	22-1096	DIODE, DUAL, BAV99	18324	BAV99
IC2	22-4292	IC, NON-INVERTING HEX BUS DRIVER	01295	HA-741CD
IC3	22-4514	IC, QUAD 2-INPUT GATE	04713	MC10102
IC4	22-4582	IC, QUAD 21/P NAND GATE	04713	74LS132

19-1164 - REFERENCE FREQUENCY MULTIPLIER ASSY (CONT'D) 2

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
Q1	22-6197	TRANSISTOR, NPN	22119	FMMT3904
Q2	22-6199	TRANSISTOR, PNP	22119	FMMT3906
Q3	22-6199	TRANSISTOR, PNP	22119	FMMT3906
Q4	22-6197	TRANSISTOR, NPN	22119	FMMT3904
Q5	22-6197	TRANSISTOR, NPN	22119	FMMT3904
Q6	22-6197	TRANSISTOR, NPN	22119	FMMT3904
Q7	22-6197	TRANSISTOR, NPN	22119	FMMT3904
R1	20-5785	RES, CHIP, 220 OHM, 1/8W, 5%	18324	RC-01
R2	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R3	20-5802	RES, CHIP, 12K, 1/8W, 5%	18324	RC-01
R4	20-5795	RES, CHIP, 1.8K, 1/8W, 5%	18324	RC-01
R5	20-5813	RES, CHIP, 100K, 1/8W, 5%	18324	RC-01
R6	20-5817	RES, CHIP, 560K, 1/8W, 5%	18324	RC-01
R7	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R8	20-5796	RES, CHIP, 2.2K, 1/8W, 5%	18324	RC-01
R9	20-5796	RES, CHIP, 2.2K, 1/8W, 5%	18324	RC-01
R10	20-5789	RES, CHIP, 560 OHM, 1/8W, 5%	18324	RC-01
R11	20-5795	RES, CHIP, 1.8K, 1/8W, 5%	18324	RC-01
R12	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R13	20-5796	RES, CHIP, 2.2K, 1/8W, 5%	18324	RC-01
R14	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R15	20-5768	RES, CHIP, 10K, 1/8W, 5%	18324	RC-01
R16	20-5791	RES, CHIP, 820 OHM, 1/8W, 5%	18324	RC-01
R17	20-5779	RES, CHIP, 56 OHM, 1/8W, 5%	18324	RC-01

19-1164 - REFERENCE FREQUENCY MULTIPLIER ASSY (CONT'D) 2

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R18	20-5787	RES, CHIP, 330 OHM, 1/8W, 5%	18324	RC-01
R19	20-5795	RES, CHIP, 1.8K, 1/8W, 5%	18324	RC-01
R20	20-5779	RES, CHIP, 56 OHM, 1/8W, 5%	18324	RC-01
R21	20-5779	RES, CHIP, 56 OHM, 1/8W, 5%	18324	RC-01
R22	20-5791	RES, CHIP, 820 MFD, 1/8W, 5%	18324	RC-01
R23	20-5795	RES, CHIP, 1.8K, 1/8W, 5%	18324	RC-01
R24	20-5795	RES, CHIP, 1.8K, 1/8W, 5%	18324	RC-01
R25	20-5795	RES, CHIP, 1.8K, 1/8W, 5%	18324	RC-01
R26	20-5795	RES, CHIP, 1.8K, 1/8W, 5%	18324	RC-01
R27	20-5785	RES, CHIP, 220 OHM, 1/8W, 5%	18324	RC-01
R28	20-5785	RES, CHIP, 220 OHM, 1/8W, 5%	18324	RC-01
R29	20-5785	RES, CHIP, 220 OHM, 1/8W, 5%	18324	RC-01
R30	20-5785	RES, CHIP, 220 OHM, 1/8W, 5%	18324	RC-01
R31	20-5785	RES, CHIP, 220 OHM, 1/8W, 5%	18324	RC-01
SK16	23-5167	CONNECTOR, 10 WAY	21793	23-5167
SK17	23-5166	CONNECTOR, 5 WAY	21793	23-5166
T1	17-3226	TRANSFORMER	21793	17-3226
TP1	24-3537	TEST POINT	21793	24-3537
XL1	17-2114	CRYSTAL, 10 MHZ	21793	17-2114

404398 - OPTION 41, CHANNEL C A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	404389	PCB ASSY., CHANNEL C	21793	404389
3	601235	CONNECTOR, BNC, PNL MTG	21793	601235
5	610777	CABLE TIE	53421	T18R
7	611067	SCREW, METRIC, M3 X 8 (2 REQ'D)	---	---
9	617102	WASHER, FLAT, #4, LIGHT SERIES (2 REQ'D)	---	---
10	617127	WASHER, LOCK, #4, LIGHT SERIES (2 REQ'D)	---	---

404389, CHANNEL "C" ASSY., 1.3 GHZ

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C1	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C2	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C3	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C4	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C5	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C6	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C7	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C8	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C9	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C10	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C11	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C12	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C13	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C14	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C15	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C16	R-21-0795	CAP,ALUM. ELEC., 47 UF, 25V WKG, -10 +50%	54473	ECEA1HK2R2E
C17	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C18	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C19	R-21-1783	CAP, CHIP, 4.7 PF, 50V, ±.25 PF	95275	VJ1206A4R7CXA
C21	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C22	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C23	R-21-1799	CAP, CHIP, 12 PF, 50V, 5%	95275	VJ1206A391JXA
C24	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA

404389, CHANNEL "C" ASSY., 1.3 GHZ (CONT'D)

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C25	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C26	R-21-1800	CAP, CHIP, 1 NF, 50V, 20%	95275	VJ1206Y102MXA
C27	R-21-0795	CAP, ALUM. ELEC., 47 UF	54473	ECEA1HK2R2E
C28	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C29	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C30	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C31	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C32	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C33	R-21-1784	CAP, CHIP, 5.6 PF, 50V, ±.25 PF	95275	VJ1206A5R6CXA
C34	R-21-1785	CAP, CHIP, 6.8 PF, 50V, ±.25 PF	95275	VJ1206A6R8CXA
C35	R-21-1785	CAP, CHIP, 6.8 PF, 50V, ±.25 PF	95275	VJ1206A6R8CXA
C36	R-21-1785	CAP, CHIP, 6.8 PF, 50V, ±.25 PF	95275	VJ1206A6R8CXA
C37	R-20-1795	CAP, CHIP, 47 PF, 50V, 5%	95275	VJ1206A470JXA
C38	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C39	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C40	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C41	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C42	R-21-1784	CAP, CHIP, 5.6 PF, 50V, ±.25 PF	95275	VJ1206A5R6CXA
C43	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C44	R-21-0795	CAP, ALUM. ELEC., 47 UF	54473	ECEA1HK2R2E
C45	R-21-0704	CAP, ALUM. ELEC., 47 UF	18324	122-53479
C46	R-21-1782	CAP, CHIP, 3.9 PF, 50V, ±.25 PF	95275	VJ1206A3R9CXA
C47	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C48	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA

404389, CHANNEL "C" ASSY., 1.3 GHZ (CONT'D)

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C49	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C50	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C51	R-21-1789	CAP, CHIP, 15 PF, 50V, 5%	95275	VJ1206A150JXA
C52	R-21-1789	CAP, CHIP, 15 PF, 50V, 5%	95275	VJ1206A150JXA
C53	100133	CAP, CERAM, .1 UF, 20%, LP	72982	8131LP-100-651-104M
D1	210089	DIODE, SILICO	50434	5082-2835
D2	R-22-1058	DIODE, SILICO	50434	5082-3379
D3	210089	DIODE, SILICO	50434	5082-2835
D5	210089	DIODE, SILICO	50434	5082-2835
D6	210089	DIODE, SILICO	50434	5082-2835
D7	R-22-1058	DIODE, SILICO	50434	5082-3379
D8	210017	DIODE, HOT CARRIER, MATCHED PAIR	21793	210017
D9	210017	DIODE, HOT CARRIER, MATCHED PAIR	21793	210017
D10	R-22-1814	DIODE, ZENER	22119	BZX79C9V1
D11	R-22-1814	DIODE, ZENER	22119	BZX79C9V1
D12	R-22-1029	DIODE, SILICO	14433	1N4149
IC1	230547	IC, QUAD COMPARATOR	27014	LM339N
IC2	230787	IC, TRIPLE LINE RECEIVER	04713	MC10116P
IC3	R-22-4694	IC, 1.3 GHz PRESCALER PLESSEY	52648	SP4730
IC4	230193	IC, TTL LOW POWER SHOTTY NAND GATES	01295	74LS00
L1	R-17-3240	COIL ASSY	21793	R-17-3240

404389, CHANNEL "C" ASSY., 1.3 GHZ (CONT'D)

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
Q1	R-22-6123	TRANSISTOR	34553	BFR90
Q2	R-22-6123	TRANSISTOR	34553	BFR90
Q3	R-22-6123	TRANSISTOR	34553	BFR90
Q4	R-22-6155	TRANSISTOR	50434	HXTR3101
R3	R-20-5768	RES, CHIP, 10K, 1/8W, 5%	65940	MCR18-10K-5PCT
R4	R-20-5768	RES, CHIP, 10K, 1/8W, 5%	65940	MCR18-10K-5PCT
R5	R-20-5841	RES, CHIP, 150 OHM, 1W	56235	2021CPX151J
R6	R-20-5837	RES, CHIP, 39 OHM, 1W	56235	2021CPX390J
R7	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R8	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5%, 200V	65940	MCR18-150-5PCT
R9	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R10	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	65940	MCR18-100-5PCT
R11	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R12	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT
R13	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5%, 200V	65940	MCR18-33-5PCT
R14	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R15	R-20-5786	RES, CHIP, 270 OHM, 1/8W, 5%, 200V	65940	MCR18-270-5PCT
R16	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5%, 200V	65940	MCR18-390-5PCT
R18	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT
R19	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5%, 200V	65940	MCR18-33-5PCT
R20	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R21	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5%, 200V	65940	MCR18-180-5PCT
R22	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5%, 200V	65940	MCR18-180-5PCT
R23	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5%, 200V	65940	MCR18-390-5PCT
R24	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT

404389, CHANNEL "C" ASSY., 1.3 GHZ (CONT'D)

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R25	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5%, 200V	65940	MCR18-33-5PCT
R26	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R27	R-20-7049	POT, 20K	73138	72XLR20K
R28	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5%, 200V	06540	MCR18-390-5PCT
R29	R-20-5813	RES, CHIP, 100K, 1/8W, 5%, 200V	06540	MCR18-100K-5PCT
R30	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	06540	MCR18-10-5PCT
R31	R-20-5774	RES, CHIP, 22 OHM, 1/8W, 5%, 200V	06540	MCR18-22-5PCT
R32	R-20-5785	RES, CHIP, 220 OHM, 1/8W, 5%, 200V	06540	MCR18-220-5PCT
R33	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5%, 200V	06540	MCR18-1.5K-5PCT
R34	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5%, 200V	06540	MCR18-1.5K-5PCT
R35	R-20-5810	RES, CHIP, 56K, 1/8W, 5%, 200V	06540	MCR18-56K-5PCT
R36	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	06540	MCR18-10-5PCT
R37	R-20-5779	RES, CHIP, 56 OHM, 1/8W, 5%, 200V	06540	MCR18-56-5PCT
R38	R-20-5810	RES, CHIP, 56K, 1/8W, 5%, 200V	06540	MCR18-56K-5PCT
R39	R-20-5770	RES, CHIP, 1M, 1/8W, 5%, 200V	06540	MCR18-1M-5PCT
R41	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5%, 200V	06540	MCR18-4.7K-5PCT
R42	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5%, 200V	06540	MCR18-4.7K-5PCT
R44	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	06540	MCR18-1K-5PCT
R45	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5%, 200V	06540	MCR18-150-5PCT
R46	R-20-5775	RES, CHIP, 27 OHM, 1/8W, 5%, 200V	06540	MCR18-27-5PCT
R47	R-20-5775	RES, CHIP, 27 OHM, 1/8W, 5%, 200V	06540	MCR18-27-5PCT
R48	R-20-5775	RES, CHIP, 27 OHM, 1/8W, 5%, 200V	06540	MCR18-27-5PCT
R49	R-20-5775	RES, CHIP, 27 OHM, 1/8W, 5%, 200V	06540	MCR18-27-5PCT
R50	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5%, 200V	06540	MCR18-470-5PCT

404389, CHANNEL "C" ASSY. 1.3 GHZ (CONT'D)

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R52	R-20-5801	RES, CHIP, 6.8K, 1/8W, 5%, 200V	06540	MCR18-6.8K-5PCT
R53	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5%, 200V	06540	MCR18-3.3K-5PCT
R54	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	06540	MCR18-1K-5PCT
R55	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R56	R-20-5790	RES, CHIP, 680 OHM, 1/8W, 5%, 200V	65940	MCR18-680-5PCT
R57	R-20-5766	RES, CHIP, 2.7K, 1/8W, 5%	65940	MCR18-2.7K-5PCT
R58	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5%, 200V	65940	MCR18-3.3K-5PCT
R59	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R60	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R61	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R62	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R66	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5%	65940	MCR18-150-5PCT
R68	R-20-5770	RES, CHIP, 1M, 1/8W, 5%	65940	MCR18-1M-5PCT
R69	R-20-5770	RES, CHIP, 1M, 1/8W, 5%	65940	MCR18-1M-5PCT
R70	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT
R71	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT
SK7	R-23-5173	CONNECTOR, 30 WAY	21793	R-23-5173
3	601257	CABLE ASSEMBLY	19505	80-1151-1425
4	601256	CONNECTOR	19505	2009-7511-000
6	R-13-2103	SCREEN (2 REQ'D)	21793	R-13-2103
7	R-13-2104	COVER (2 REQ'D)	21793	R-13-2104
8	R-14-4000	SPACER (2 REQ'D)	21793	R-14-4000
10	R-18-1142	P.C. BOARD (UNLOADED)	21793	R-18-1142
156	617042	NUT, HEX, M3 (2 REQ'D)	1CJ86	DIN934-ME
158	R-24-2801	WASHER, CRINKLE, M3 (2 REQ'D)	21793	R-24-2801
166	500022	WIRE, BARE COPPER/TIN, 22GA	21793	500022

Racal Instruments

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RACAL

RACAL-DANA Instruments Inc. *4 Goodyear Street, Irvine, California 92718-2202*

REPAIR AND CALIBRATION REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Racal-Dana Repair Facility.

Model No_____ Serial No_____ Date_____

Company Name_____ P.O. No_____

Billing Address_____

City State Zip

Shipping Address_____

City State Zip

Technical Contact_____ Phone Number (___)_____

Purchasing Contact_____ Phone Number (___)_____

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

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2. If problem is occurring when unit is in remote, please list the program strings used and the controller type.

_____

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3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.).

_____

_____

_____

4. Is calibration data required? Yes No (circle one)

Call for RMA No. before shipping: Customer Service
(714) 859-8999 x230 OR 1 (800) RAC-DANA

Ship instrument to: Customer Service Department
Racal-Dana Instruments Inc.
4 Goodyear Street
Irvine, CA 92718

Note: We do not accept "collect" shipments.

MP MASTER
MA31103